NIKO-SEM

N- & P-Channel Enhancement Mode Field Effect Transistor_Preliminary

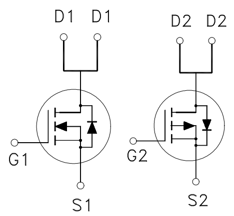
P5003QVG

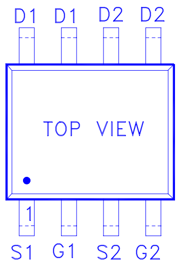
SOP-8

Lead-Free

PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
N-Channel	30	27.5mΩ	7A
P-Channel	-30	45mΩ	-5A





G : GATE
D : DRAIN
S : SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	N-Channel	P-Channel	UNITS
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	7	-5	A
	T_C = 70 °C		6	-4	
Pulsed Drain Current[1]		I_{DM}	20	-20	
Power Dissipation	T_C = 25 °C	P_D	2		W
	T_C = 70 °C		1.3		
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		62.5	°C / W

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	N-Ch	30			V
		V_{GS} = 0V, I_D = -250µA	P-Ch	-30			
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	N-Ch	1	1.5	2.5	
		V_{DS} = V_{GS}, I_D = -250µA	P-Ch	-1	-1.5	-2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V	N-Ch			±100	nA
		V_{DS} = 0V, V_{GS} = ±20V	P-Ch			±100	

Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V, V_{GS} = 0V	N-Ch			1	µA
		V_{DS} = -24V, V_{GS} = 0V	P-Ch			-1	
		V_{DS} = 20V, V_{GS} = 0V, T_J = 55 °C	N-Ch			10	
		V_{DS} = -20V, V_{GS} = 0V, T_J = 55 °C	P-Ch			-10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	N-Ch	20			A
		V_{DS} =-5V, V_{GS} = -10V	P-Ch	-20			
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 6A	N-Ch		30	40	mΩ
		V_{GS} = -4.5V, I_D = -5A	P-Ch		62	80	
		V_{GS} = 10V, I_D = 7A	N-Ch		20.5	27.5	
		V_{GS} = -10V, I_D = -6A	P-Ch		37.5	45	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 7A	N-Ch		16		S
		V_{DS} = -5V, I_D = -6A	P-Ch		13		

DYNAMIC							
Input Capacitance	C_{iss}	N-Channel V_{GS} = 0V, V_{DS} = 15V, f = 1MHz P-Channel V_{GS} = 0V, V_{DS} = -15V, f = 1MHz	N-Ch		680		pF
			P-Ch		920		
Output Capacitance	C_{oss}		N-Ch		105		
			P-Ch		190		
Reverse Transfer Capacitance	C_{rss}		N-Ch		75		
			P-Ch		120		
Total Gate Charge[2]	Q_g	N-Channel V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = 10V, I_D = 7A P-Channel V_{DS} = 0.5$V_{(BR)DSS}$, V_{GS} = -10V, I_D = -6A	N-Ch		14		nC
			P-Ch		18.5		
Gate-Source Charge[2]	Q_{gs}		N-Ch		1.9		
			P-Ch		2.7		
Gate-Drain Charge[2]	Q_{gd}		N-Ch		3.3		
			P-Ch		4.5		
Turn-On Delay Time[2]	$t_{d(on)}$	N-Channel V_{DD} = 10V I_D ≅ 1A, V_{GS} = 10V, R_{GEN} = 3Ω P-Channel V_{DD} = -10V I_D ≅ -1A, V_{GS} = -10V, R_{GEN} = 3Ω	N-Ch		4.6	7	nS
			P-Ch		7.7	11.5	
Rise Time[2]	t_r		N-Ch		4	6	
			P-Ch		5.7	8.5	
Turn-Off Delay Time[2]	$t_{d(off)}$		N-Ch		20	30	
			P-Ch		20	30	
Fall Time[2]	t_f		N-Ch		5	8	
			P-Ch		9.5	14	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)							
Continuous Current	I_S		N-Ch			1.3	A
			P-Ch			-1.3	
Pulsed Current[3]	I_{SM}		N-Ch			2.6	
			P-Ch			-2.6	
Forward Voltage[1]	V_{SD}	I_F = 1A, V_{GS} = 0V	N-Ch			1	V
		I_F = -1A, V_{GS} = 0V	P-Ch			-1	

[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P5003QVG", DATE CODE or LOT #

Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

SOIC-8(D) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.5	0.715	0.83
B	3.8	3.9	4.0	I	0.18	0.254	0.25
C	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	K	0°	4°	8°
E		1.27		L			
F	1.35	1.55	1.75	M			
G	0.1	0.175	0.25	N