MS-7581

Ver: 0A

uATX(244mm X 244mm)

CPU:

INTEL -HAVENDALE/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:IDT 4100

HD Audio Codec:RTL889

LAN:Intel integrated Hanksville 10/100/1000 NIC

SIO:FIN71889

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X8) Slot * 1
PCI Express (X1) Slot * 1
PCI Slot * 1

PWM:

Controller:ISL6334 (4-Phase 95W)
Controller:ISL

ACPI:

INTERSIL

Other:

SATA(SATA2-300MB/s) *4
USB2.0 *14 (Rear*6 Front*4 Intrenal *4)
DISPLAY PORT*1
VGA PORT *1
PRINT Header *1
COM PORT *1
COM Header *1

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Size: Custom | Document Description: Cover Sheet | Rev: 0A

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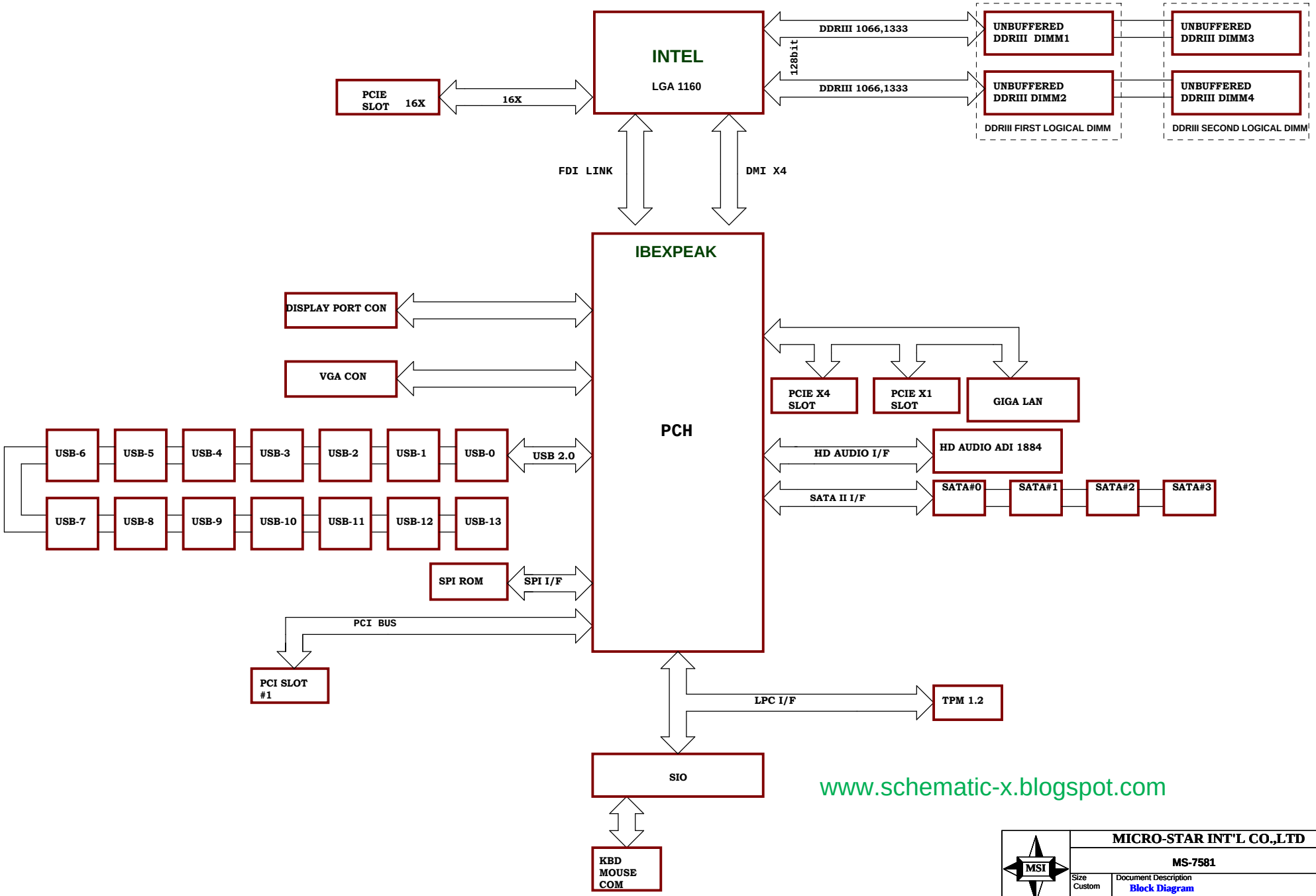

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Size	Document Description	Rev
Custom	Block Diagram	0A

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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MA0_CLK_H0/L0 MEM_MA0_CLK_H1/L1 MEM_MA0_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MB0_CLK_H0/L0 MEM_MB0_CLK_H1/L1 MEM_MB0_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

PCI Config.

DEVICE	MCP1 INT Pin	REQ# / GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD16	CLK33M_PCISLOT_J20
TPM				LPCCLK0
SIO				LPCCLK1

TABLE 9
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #x	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

IBEXPEAK GPIO DEFINITION						
Pin	GPIO	POWER WELL	I/O	Function	Implementation	Function
AK41	GPIO0	MAIN	I	BMBUSY#	Pull-up to +3.3V and connect to the PECI_REQ# pin (TBD) on the SIO	PECI_REQ#
AL14	GPIO1	MAIN	I	TACH1	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH1
AU8	GPIO2	MAIN	I	PCI_IRQE#	See PCA Spec	PCI Interrupt E#
AH7	GPIO3	MAIN	I	PCI_IRQF#	See PCA Spec	PCI Interrupt F#
AP12	GPIO4	MAIN	I	PCI_IRQG#	See PCA Spec	PCI Interrupt G#
AW4	GPIO5	MAIN	I	PCI_IRQH#	See PCA Spec	PCI Interrupt H#
AV11	GPIO6	MAIN	I	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMM B assembly connects pin 12 directly to GND	COMM_B_DET#
AY11	GPIO7	MAIN	I	TACH3	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH3
AK30	GPIO8	RESUME	O	ICC_EN#		Reserved
AL28	GPIO9	RESUME	I	OC5	Associated with USB port 05 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#
AL30	GPIO10	RESUME	I	OC6	Pull-up to +3_3VSB and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
AL31	GPIO11	RESUME	I	SMBALERT#	Pull-up to +3_3VSB. It is always enabled as a wake event.	SMBALERT#
AU34	GPIO12	RESUME	I	LAN_DISABLE	Follow implementation in Intel Pickton Design Guide	LAN_DISABLE#
AR16	GPIO13	RESUME	I	IO_PME	Pull-up to +3_3V SB and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET# or DASH_SMI
AM30	GPIO14	RESUME	I	OC7	Pull-up to +3.3VSB and connect to the SMI pin on the SIO	SMI#from SIO
AY36	GPIO15	RESUME	I	PCH_GPI15		Reserved
AH39	GPIO16	RESUME	O	SATA4GP	Follow implementation in Intel Pickton Design Guide	CPU_MISSING
AW11	GPIO17	MAIN	I	TACH0	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH0
AM39	GPIO18	MAIN	I	PCICLKRQ1#	Through a 1KΩ series resistor, pull-up to +3.3V and connect to E15-pin 1.	BOOT_BLK_REC#
AH38	GPIO19	MAIN	I	SATA1GP	Pull-up to +3_3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID1
AP38	GPIO20	MAIN	I	PCICLKRQ2#		PCIECLKRQ2#
AJ37	GPIO21	MAIN	I	SATA0GP	Pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
AN41	GPIO22	MAIN	I	SCLOCK	Pull-up to +3_3V and connect to P150-pin 10	INT_USB_DET#
AP14	GPIO23	MAIN	I	LDRQ1#	Pull-up to +3.3V and connect to the PCI SLOT Riser Detect circuit.	RISER_DET#
AR34	GPIO24	RESUME	O	MEMLED	Through a 1kΩ series resistor, pull-up to +3_3VSB and connect to P125-Pin 1	HOOD_SW_DET#
AP33	GPIO25	RESUME	I	PCICLKRQ3#		PCIECLKRQ3#
AW37	GPIO26	RESUME	I	PCICLKRQ4#		PCIECLKRQ4#
AP37	GPIO27	RESUME	O	OD_PLL_VR_EN		Reserved
AV40	GPIO28	RESUME	O	PCH_GP28		
BA35	GPIO29	RESUME	O	SLP_LAN#	Connect to a circuit used to force the 3.3V_CL rail on.	WOL_EN
AT37	GPIO30	RESUME	I	SUS_PWR_ACK		
AP40	GPIO31	MAIN	I	ACPRESENT	TBD. For now connect to a Test Point	ESATA_DET#
AJ40	GPIO32	MAIN	O	PCH_GP32	Through a 1kΩ series resistor, pull-up to +3_3V and connect to P1-pin 20.	85%_PS_DET#
AT16	GPIO33	MAIN	O	PCH_GP33	Through a 1kΩ series resistor, pull-up to +3_3V and connect to pin 1 of jumper E1.	FDT_OVRD#
AT40	GPIO34	MAIN	O	SP_PCI#	Pull-down to GND and connect to P124-pin 2. Decouple with 0.1µF	HOOD_LOCK_DET
AR41	GPIO35	MAIN	O	SATACLKREQ#	Pull-up to +3_3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
AK39	GPIO36	MAIN	I	SATA2GP	Pull-up to +3_3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
AR38	GPIO37	MAIN	I	SATA3GP	Pull-up to +3_3V and connect to P126-pin 16	PRNTR_DET#
AM38	GPIO38	MAIN	I	SLOAD	Through a series 1K resistor, connect to P5-pin 9 and pull-up to +3_3V	CHASSIS_ID0
AL39	GPIO39	MAIN	I	SDATAOUT0	Pull-up to +3_3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BASEPAN_DET#
AT30	GPIO40	RESUME	I	OC1	Using an 8.2kΩ resistor, pull-down to GND and connect to E49-pin 2	PASSWORD_EN
AK28	GPIO41	RESUME	I	OC2	Associated with USB port 2 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#
AP30	GPIO42	RESUME	I	OC3	Associated with USB port 3 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#
AP31	GPIO43	RESUME	I	OC4	Associated with USB port 4 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#
AW38	GPIO44	RESUME	I	PCICLKRQ5#		PCIECLKRQ5#
AV36	GPIO45	RESUME	I	PCICLKRQ6#		PCIECLKRQ6#
AP36	GPIO46	RESUME	I	PCICLKRQ7#		PCIECLKRQ7#
AV39	GPIO47	RESUME	I	PEG_A_CLKRQ#		PEG_A_CLKRQ#
AG38	GPIO48	MAIN	I	SDATAOUT1	Pull-up to +3_3V and connect to P24-pin 10	FRONT_USB_DET#
AG40	GPIO49	MAIN	O	SATA5GP	Pull-up to +3_3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
AW5	GPIO50	MAIN	I	PCI_REQ#1	Use as REQ1#.	REQ1#
AK6	GPIO51	MAIN	O	PCI_GNT#1	Use as GNT1#.	GNT1#
AY4	GPIO52	MAIN	I	PCI_REQ#2	Pull-up to +3_3V	REQ2#
BA9	GPIO53	MAIN	O	PCI_GNT#2	Connect to TP	GNT2#
AH8	GPIO54	MAIN	I	PCI_REQ#3	Through a 8.2KΩ series resistor, connect to P14-pin 2 and pull-down to GND.	BOOT_BLK_EN#
AM3	GPIO55	MAIN	O	PCI_GNT#3		GNT3#
AW35	GPIO56	RESUME	I	PEG_B_CLKRQ#	Connect to circuit that controls the amplifier's output.	AUD_AMP_DIS#
AL32	GPIO57	MAIN	I	PCH_GP57	Pull-up to +3_3VSB.	TPM_PP
AV31	GPIO58	RESUME	O	SMLICLK		SML1CLK
AT31	GPIO59	RESUME	I	OC0	Associated with USB port 0 power well. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#
BA33	GPIO60	RESUME	O	SML0ALERT#		SML0ALARM
AK31	GPIO61	RESUME	O	SUS_STAT#	Power Down for external TPM	LPCPD#
AH31	GPIO62	RESUME	O	SUSCLK	SUSCLK to SIO	SUSCLK
AU36	GPIO63	RESUME	O	SLP_S5#	Connect to USB Power Control on SIO	SLP_S5#
AD10	GPIO64	MAIN	O	CLKOUTFLEX0		CLKOUTFLEX0
AK1	GPIO65	MAIN	O	CLKOUTFLEX1		CLKOUTFLEX1
AB6	GPIO66	MAIN	O	CLKOUTFLEX2		CLKOUTFLEX2
AL3	GPIO67	MAIN	O	CLKOUTFLEX3		CLKOUTFLEX3
AY34	GPIO72	RESUME	I	PCH_GP72	Through a series 1KΩ resistor, pull-up to +3.3VSB and connect to P5-pin 10.	CHASSIS_ID1
AN35	GPIO73	RESUME	I	PCIECLKRQ0#		PCIECLKRQ0#
AY32	GPIO74	RESUME	O	SML1ALERT#		SML1ALERT#
AR31	GPIO75	RESUME	O	SML1DATA		SML1DATA

SIO9 PIN ASSIGNMENT (UPDATE PENDING)			
Pin	Pin Name	Function	Implementation
1	PWRBTN#	PWRBTN#	Connect to front panel header's power button pin
2	SLP_S3#	SLP_S3#	Connect to ICH10's SLP_S3# signal
3	SLP_S5#	S4_STATE#	Connect to ICH10's S4_STATE# signal
7	PDS_EN	CPU_FAN_TACH	Connect to the CPU fan tach interface
8	COLOR	LED_PWR_COLOR	Controls the Power LED color
10	PWBTOUT#	PWRBTN_OUT#	Connect to ICH PWRBTN# input
11	PS_ON#	PS_ON#	Connect to the appropriate power supply circuit
13	BLINK_GR	LED_PWR_BLINK	Connect to P5.2 through 68 ohm series resistor.
14	SIOPME#	RING#	Connect to ICH8 RI#
17	CLAMP_CTRL	CLAMP_CNTL	Use for clamping PCA voltage rails to decrease rail decay time
28	SMB1SCL	SMB_CLK_MAIN	Connect to the clock signal of the main powered system SMBus
29	SMB2SCL	SMB_CLK_STDBY	Connect to the clock signal of the standby powered system SMBus
33	GPRST2#	PCI_EXP_RST#	Use to reset all the PCIe devices and slots
34	FANPWM2	CHAS_FAN_PWM	Connect to the Chassis Fan PWM interface
35	GPIO25	PWM_IN	Connect to the ICH10's PWM0 output - NEW for Eaglelake
36	PME_IN#	P_PME#	Connect to the PME# pin of the ICH10
37	USB_PWR#	USB_PWR#	Input to USB Power control; connect to the ICH10's SLP_S5# signal
38	3V_SW_MAIN#	3V_DUAL_CNTL	Connect to control inputs of dual rail switches
39	EVENT6#	PCI_EXP_WAKE#	Connect to WAKE# pins of PCIe devices and slots
47	PDS_EN2	PDS_EN2	Use as control signal for appropriate voltage regulators
48	CPU_PRSNT1#	SKTOCC#	Connect to SKTOCC# on CPU
49	WAKE_OUT#	ICH_WAKE#	Connect to the ICH10's WAKE# input
50	GPIE14	HOOD_LOCK#	Connect to P124 pin 1 and a 2.2K pull-up to +5V.
51	GPIOE16	HOOD_UNLOCK#	Connect to P124 pin 6 and a 2.2K pull-up to +5V.
53	AUDIO_BEEP	DIAG_BEEP	Connect to the system's integrated audio solution
54	FANPWM1	CPU_FAN_PWM	Connect to the CPU fan's PWM circuit
55	GPIO35	PECI_REQ#	Connect to the ICH10's BM_BUSY# signal - New for Eaglelake; C#/C4 support
56	HD_LED_IN#	SATA_LED#	Connect to the ICH10's SATA_LED# output signal
58	HMSCL	HLTH_MON_CLK	Connect to CLK pin on SensorBus device
59	HMSDA	HLTH_MON_DAT	Connect to DAT pin on SensorBus device
60	GPIOE10	FLPY_DRVDEN	Use in floppy implementation
61	HD_LED_OUT#	HD_LED#	Connect to the front panel HDD LED
100	SMB1SDA	SMB_DATA_MAIN	Connect to the data signal of the main powered system SMBus
101	SMB2SDA	SMB_DATA_STDBY	Connect to the data signal of the standby powered system SMBus
102	5V_USB_MAIN	5V_USB_MAIN#	Connect to the control pin of the 5V_DUAL circuit.
103	GPIOE41	PS_FAN_TACH	Where applicable, connect to power supply's fan tach circuit.
104	FANPWM3	PS_FAN_PWM	Where applicable, connect to the power supply's fan PWM circuit
105	PWRGD_01	PWRGD_30MS	Use for appropriate system board sequencing
106	PWRGD_02#	PWRGD_50MS#	Use for appropriate system board sequencing
110	FAN_TACH4	CHAS_FAN_TACH	For systems with a chassis fan, connect to the chassis fan TACH circuit
111	SMI#	LPC_SMI#	Connect to appropriate ICH10 SMI-capable GPIO; reference ICH10 GPIO matrix
120	RI2#	RI2#	Where applicable, connect to appropriate serial port pin
122	DCD2#	DCD2#	Where applicable, connect to appropriate serial port pin
123	SIN2	SIN2	Where applicable, connect to appropriate serial port pin
124	SOUT2	SOUT2	Where applicable, connect to appropriate serial port pin
125	DSR2#	DSR2#	Where applicable, connect to appropriate serial port pin
126	RTS2#	RTS2#	Where applicable, connect to appropriate serial port pin
127	CTS2#	CTS2#	Where applicable, connect to appropriate serial port pin
128	DTR_BOUT2#	DTR2#	Where applicable, connect to appropriate serial port pin

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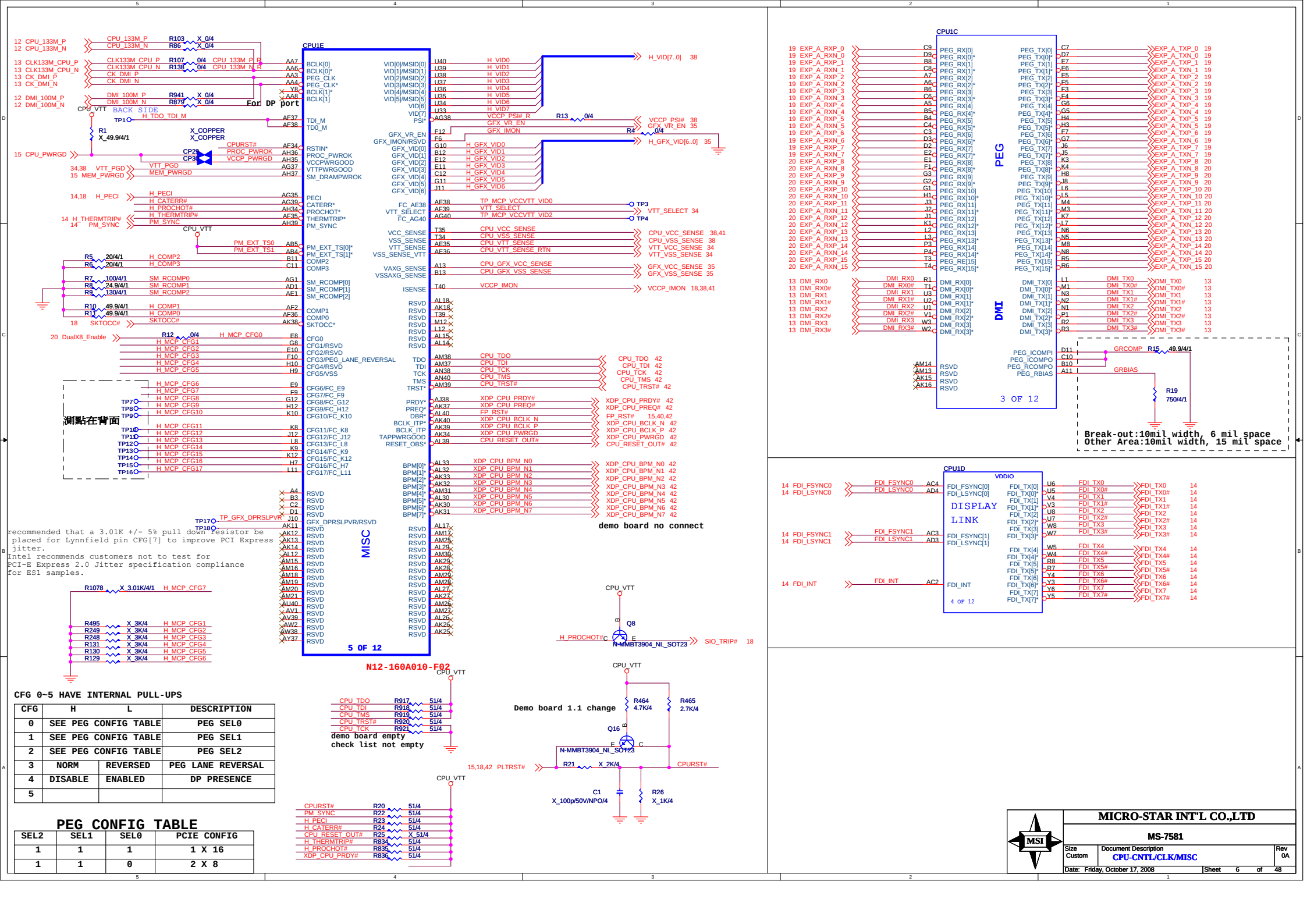

CFG 0~5 HAVE INTERNAL PULL-UPS

CFG	H	L	DESCRIPTION
0	SEE PEG CONFIG TABLE		PEG SEL0
1	SEE PEG CONFIG TABLE		PEG SEL1
2	SEE PEG CONFIG TABLE		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLED	DP PRESENCE
5			

PEG CONFIG TABLE

SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

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Size: Custom	Document Description: CPU-CNTL/CLK/MISC
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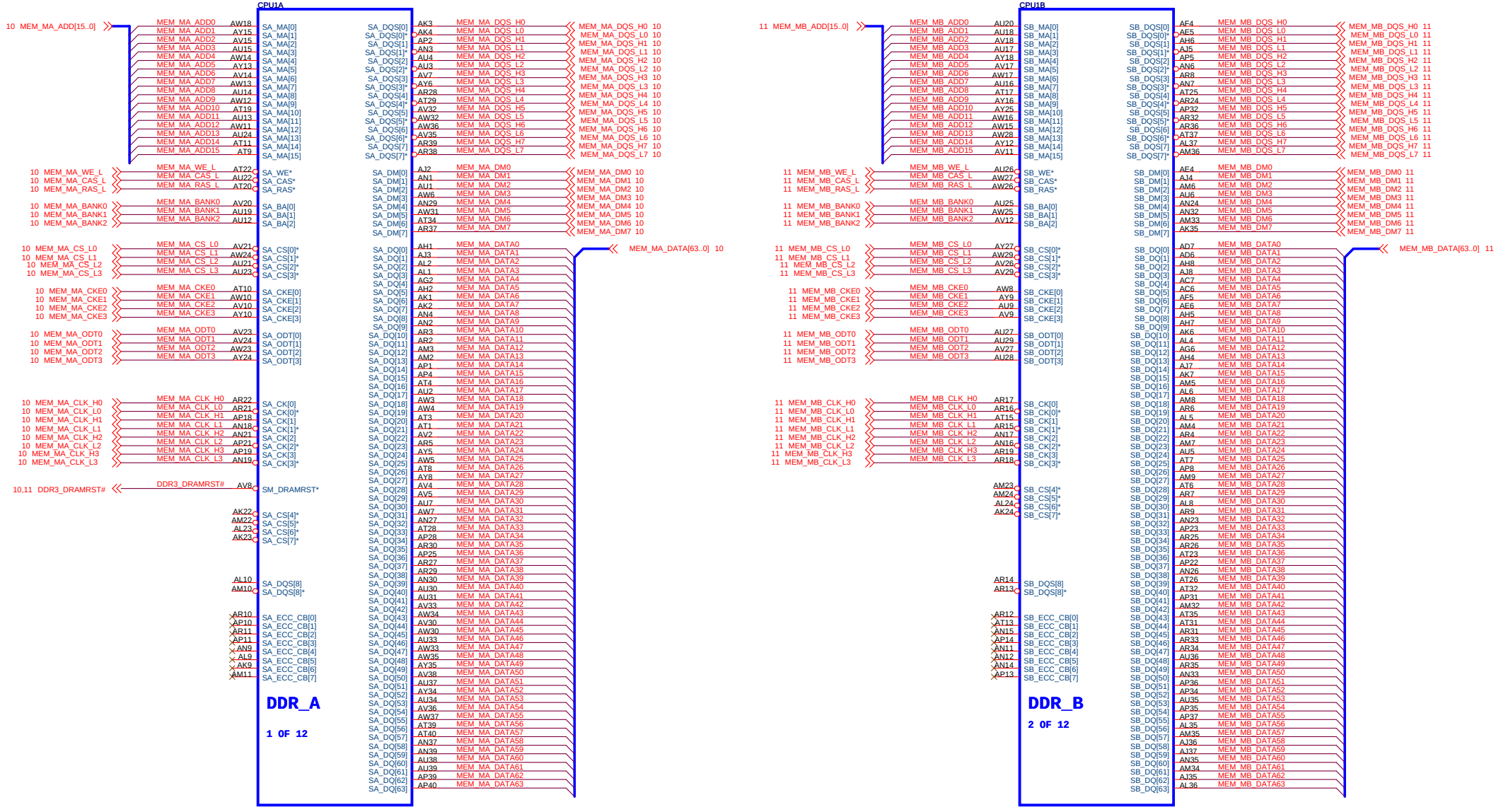
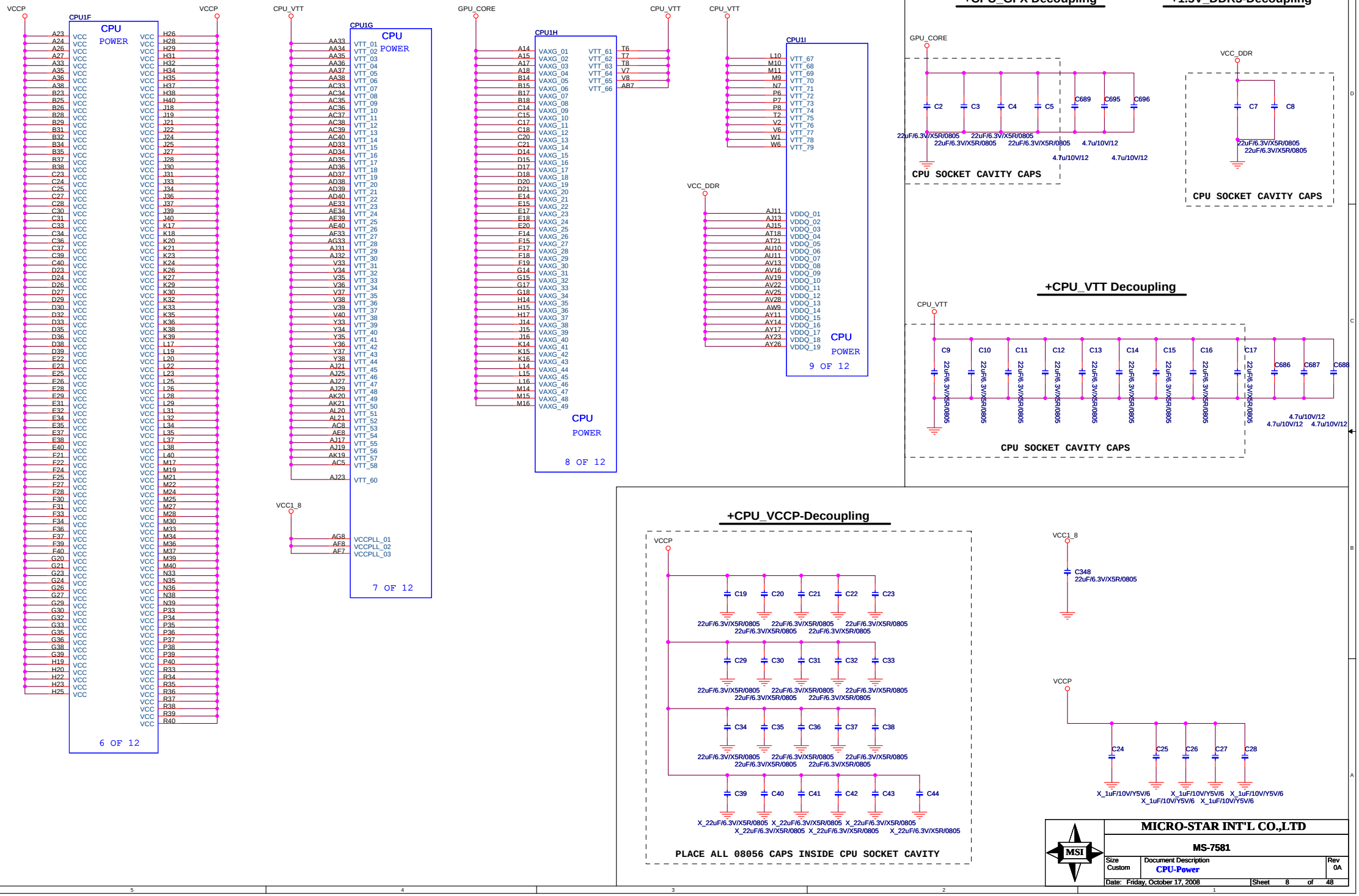

CPU1A
DDR_A
1 OF 12
CPU1B
DDR_B
2 OF 12
MEM_MA_DATA[63..0] 10
MEM_MB_DATA[63..0] 11


CPU1F
CPU
POWER
6 OF 12
CPU1G
CPU
POWER
7 OF 12
CPU1H
CPU
POWER
8 OF 12
CPU1I
CPU
POWER
9 OF 12
VCCP
CPU_VTT
GPU_CORE
VCC_DDR
VCC1_8
+CPU_GFX Decoupling
+1.5V_DDR3-Decoupling
+CPU_VTT Decoupling
+CPU_VCCP-Decoupling
CPU SOCKET CAVITY CAPS
PLACE ALL 08056 CAPS INSIDE CPU SOCKET CAVITY
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CPU-Power
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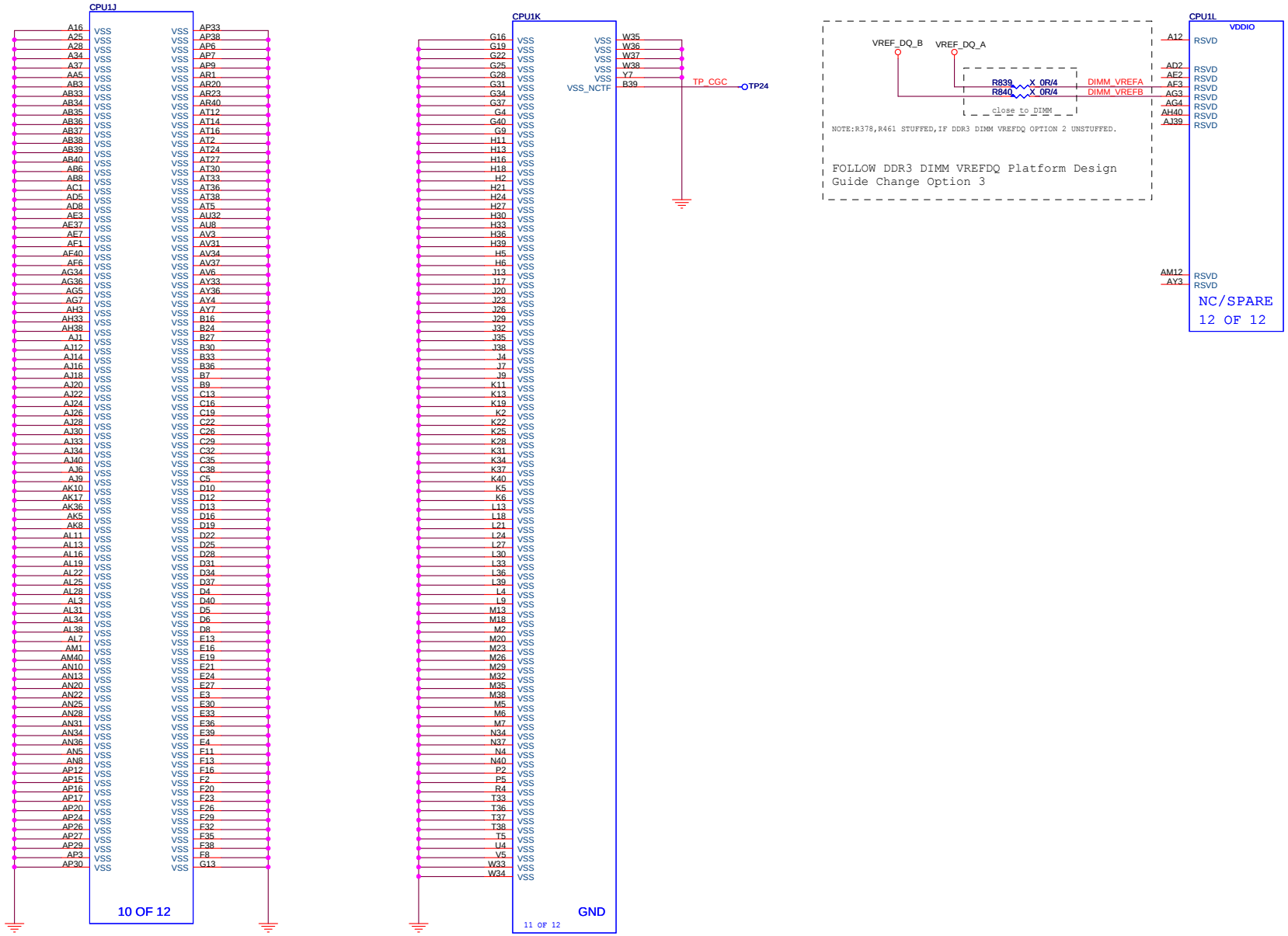

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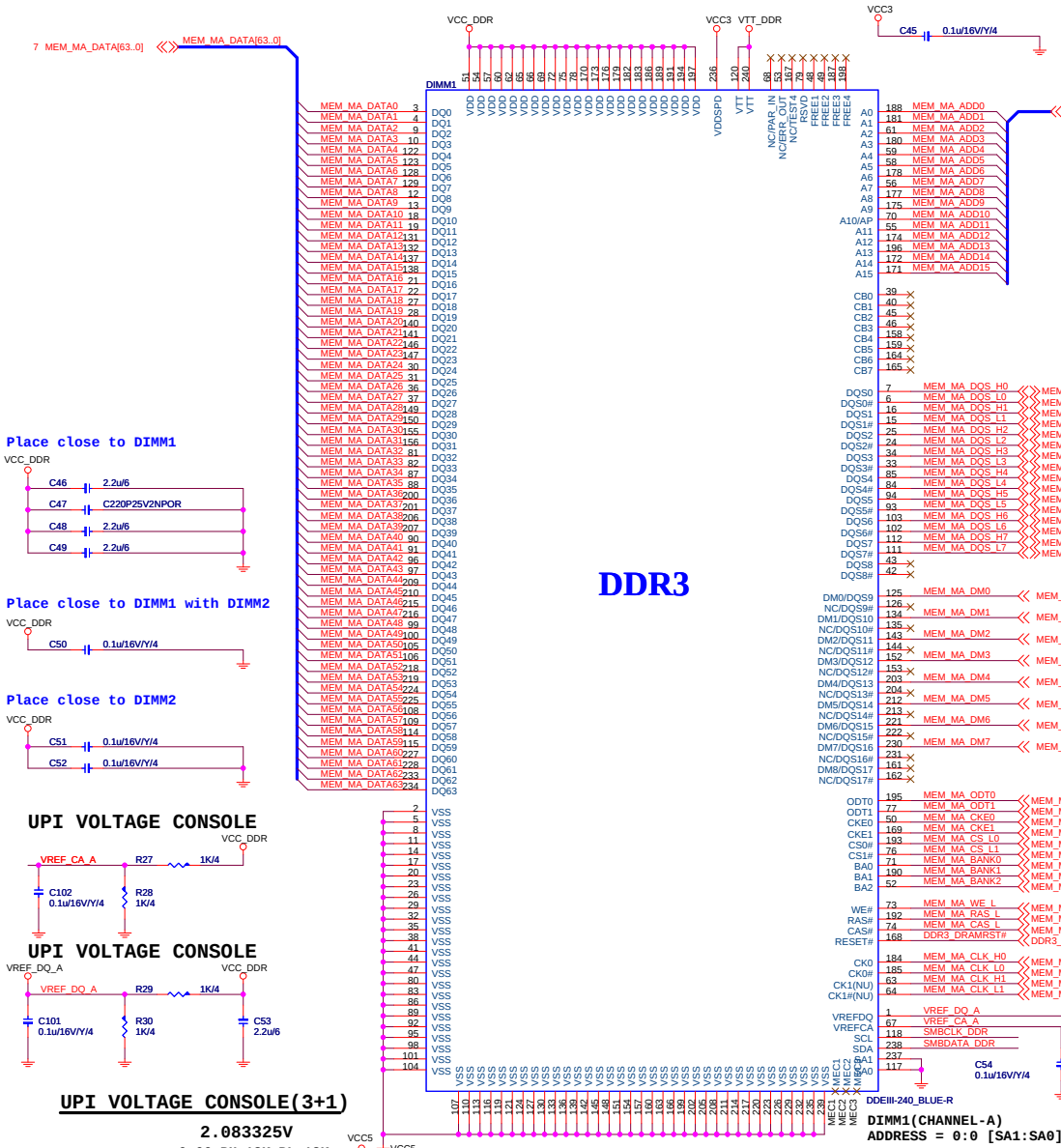
DDRIII DIMM_A1



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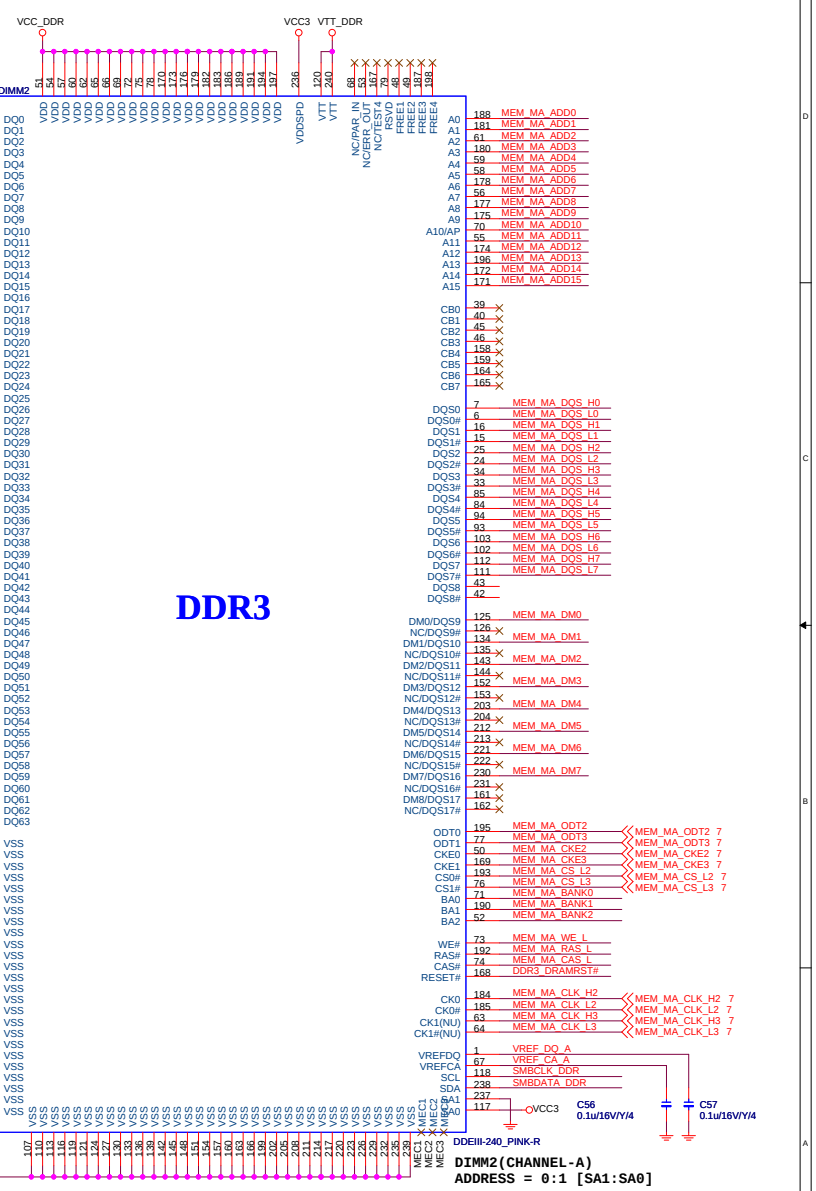

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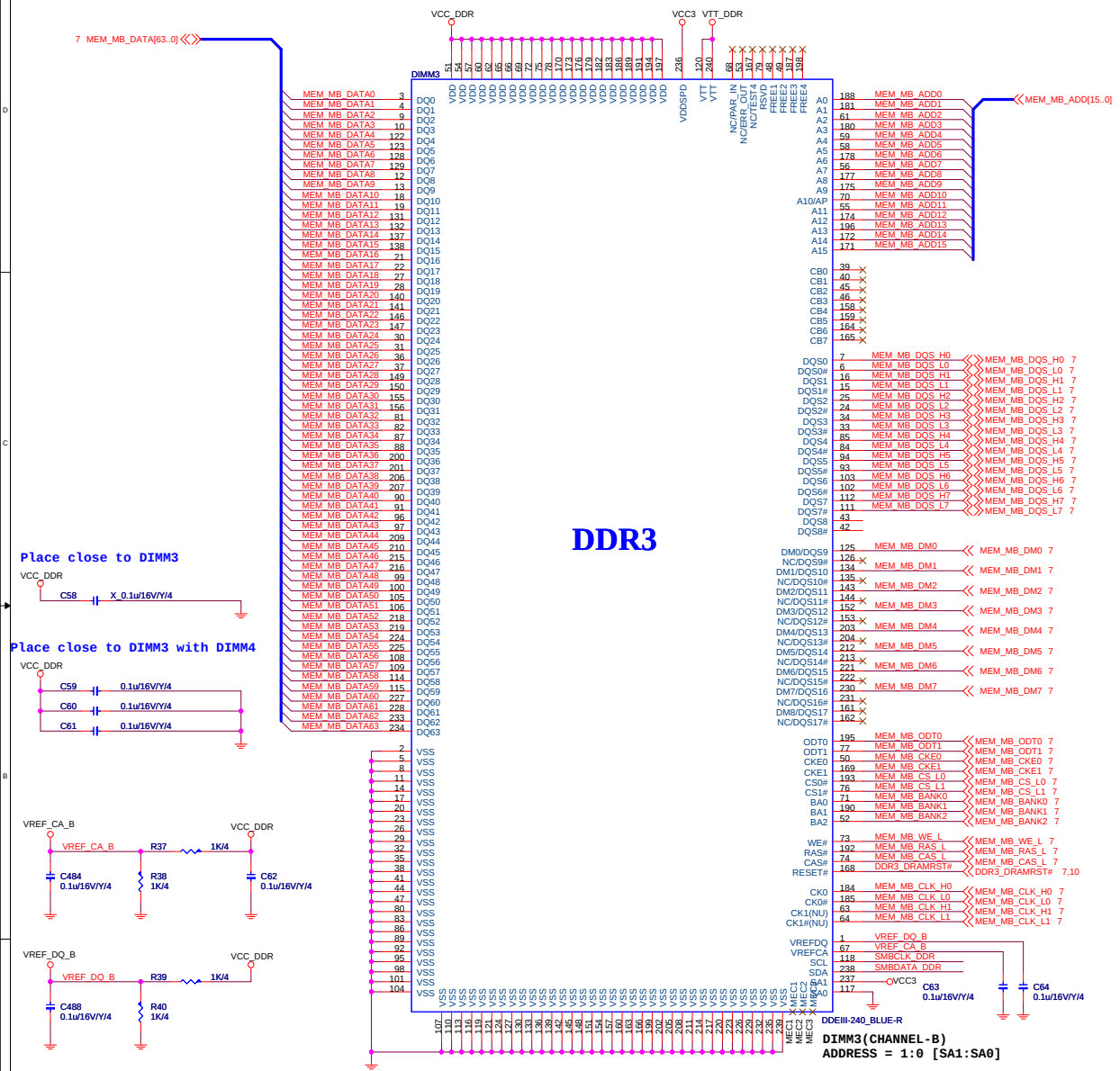
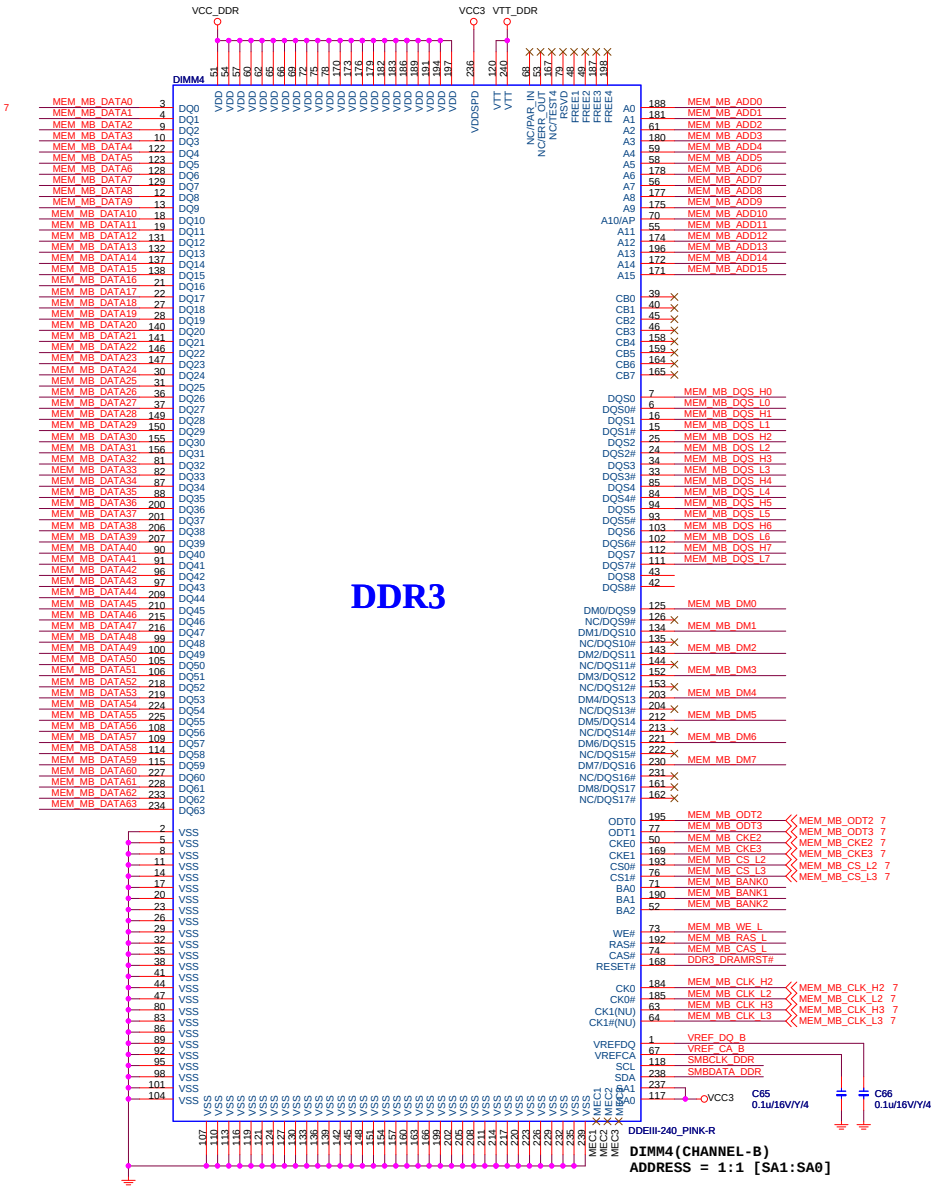
DDRIII DIMM_B1



DDRIII DIMM_B2



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

SMBCLK_DDR — SMBCLK_DDR 10

SMBDATA_DDR — SMBDATA_DDR 10

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Size: Custom	Document Description: DDR3 Chanel-B DIMM3/4 — Rev: 0A
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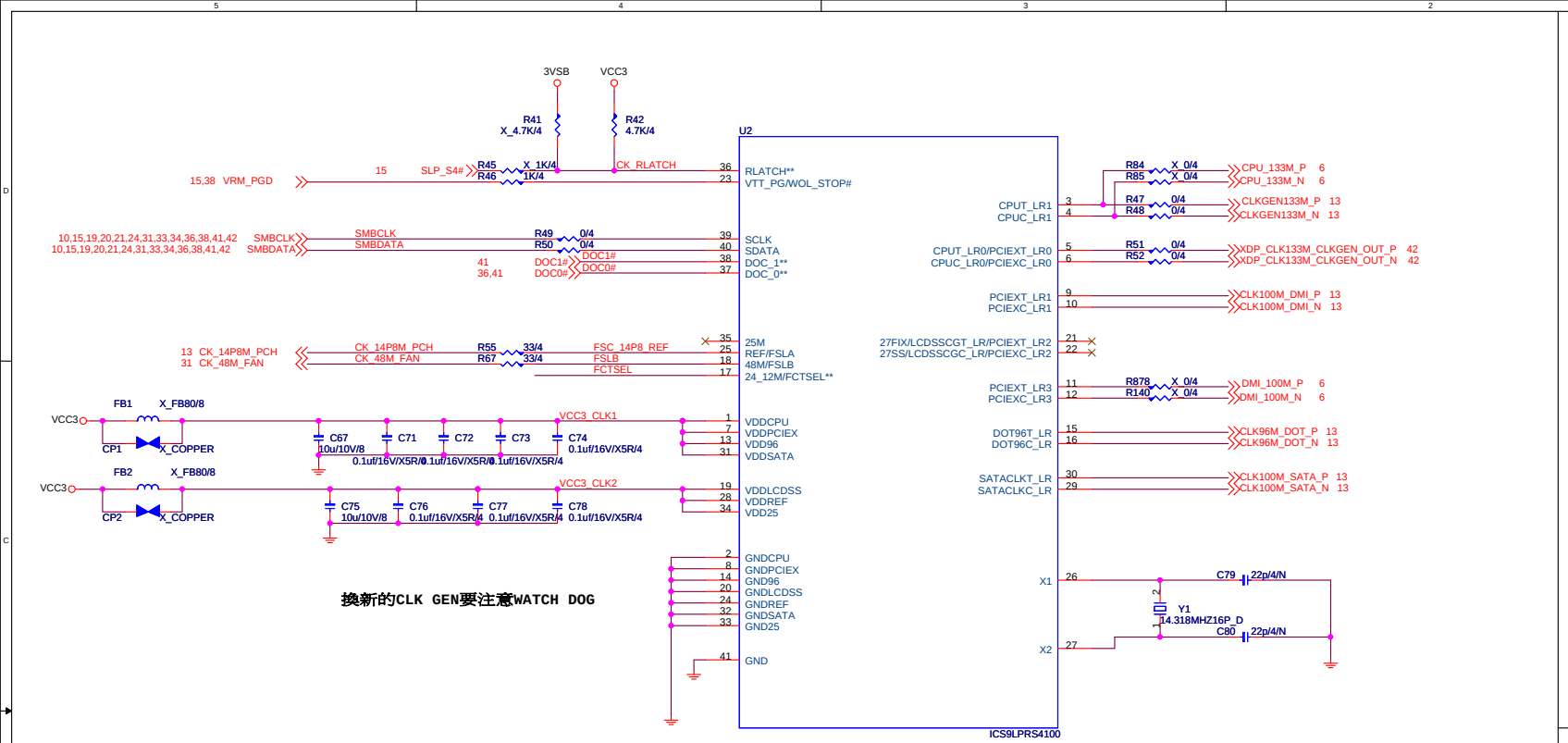
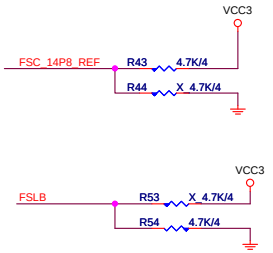


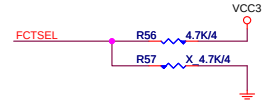
換新的CLK GEN要注意WATCH DOG

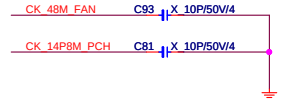
CLOCK GEN STRAPING



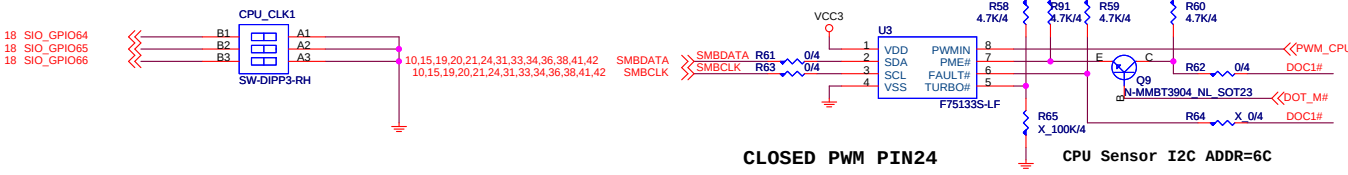
FCTSEL Functionality Table

Pin17	Pin21/22	Pin5/6
FCTSEL=0	27FIX/SS	PCIEX0
FCTSEL=M	LCD	PCIEX0
FCTSEL=1	PCIEX2	CPU0





Place near VRD11 controller as closed as possible



CLOSED PWM PIN24

CPU Sensor I2C ADDR=6C

EASY DOT FUNCTION

DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal

MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: Clock Gen ICS9LPRS4100 | Rev: 0A

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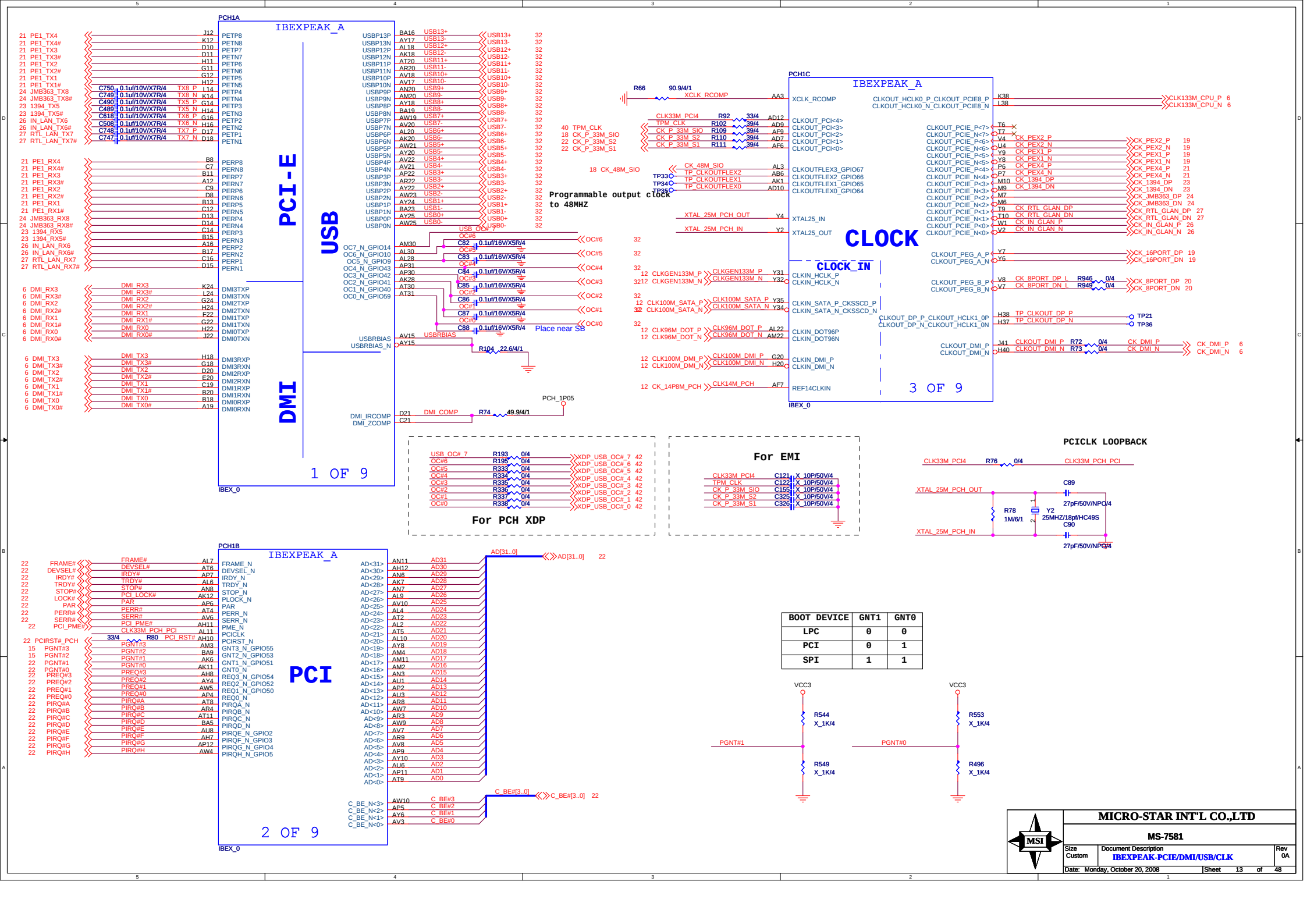
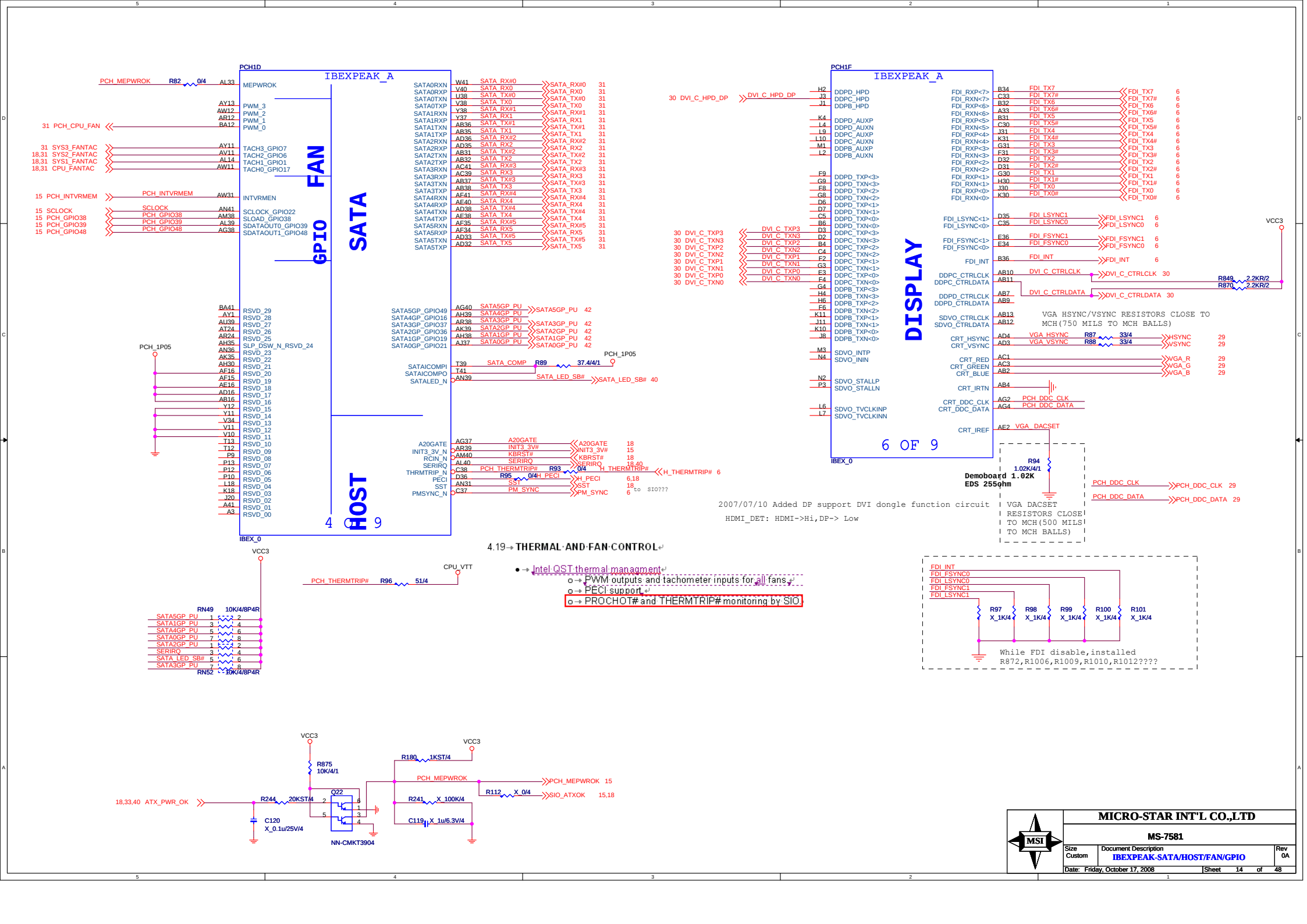


BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1


PCH1D
IBEXPEAK_A
FAN
GPIO
SATA
HOST
4 OF 9
IBEX_0
PCH1F
DISPLAY
6 OF 9
IBEX_0
2007/07/10 Added DP support DVI dongle function circuit
HDMI_DET: HDMI->Hi,DP-> Low
VGA HSYNC/VSYNC RESISTORS CLOSE TO MCH(750 MILS TO MCH BALLS)
Demoboard 1.02K
EDS 255ohm
VGA DACSET RESISTORS CLOSE TO MCH(500 MILS TO MCH BALLS)
4.19 THERMAL AND FAN CONTROL
Intel QST thermal management
PWM outputs and tachometer inputs for all fans
PECI support
PROCHOT# and THERMTRIP# monitoring by SIO
While FDI disable,installed R872,R1006,R1009,R1010,R1012????
MICRO-STAR INT'L CO.,LTD
MS-7581
IBEXPEAK-SATA/HOST/FAN/GPIO
Rev 0A
Date: Friday, October 17, 2008
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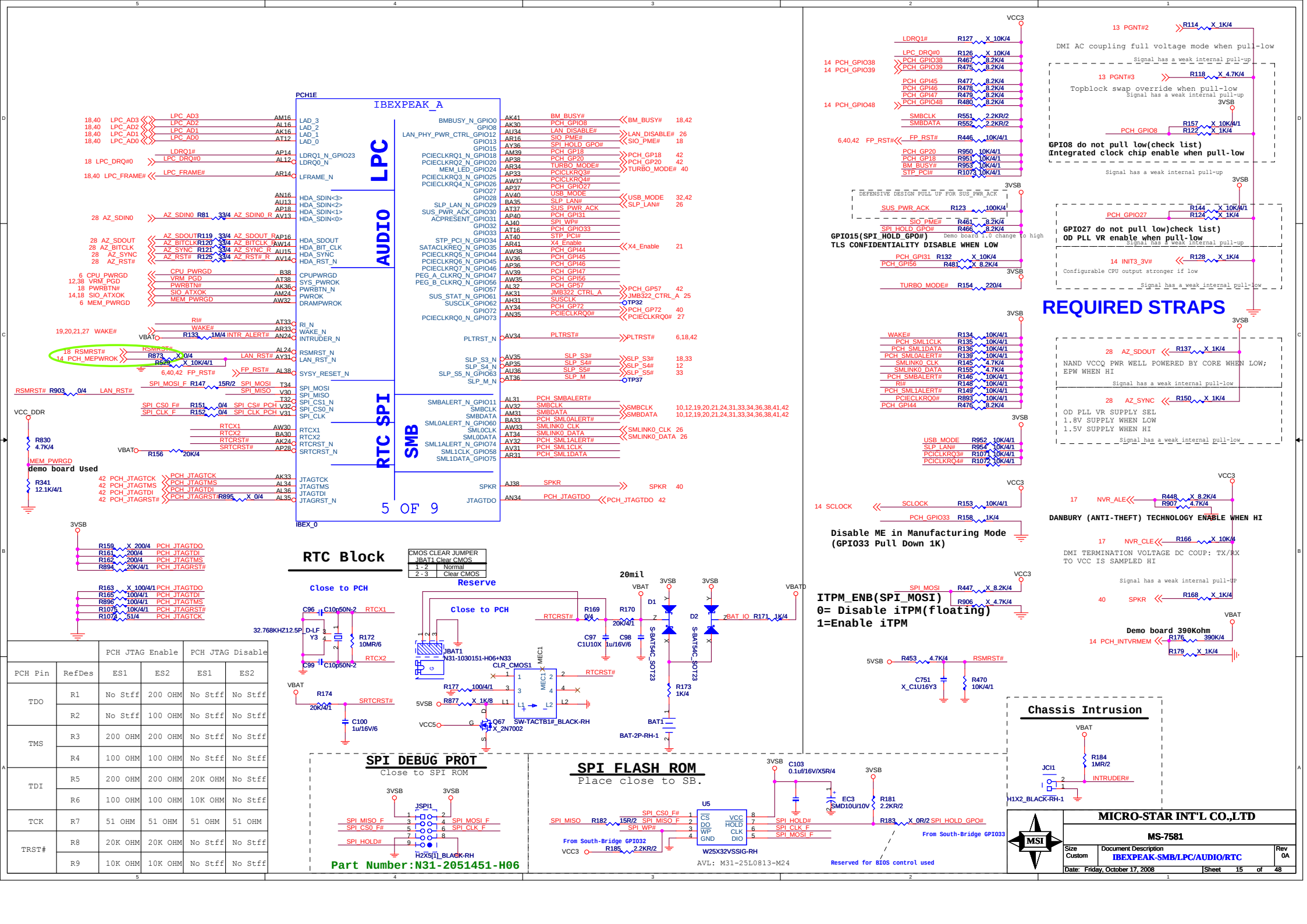
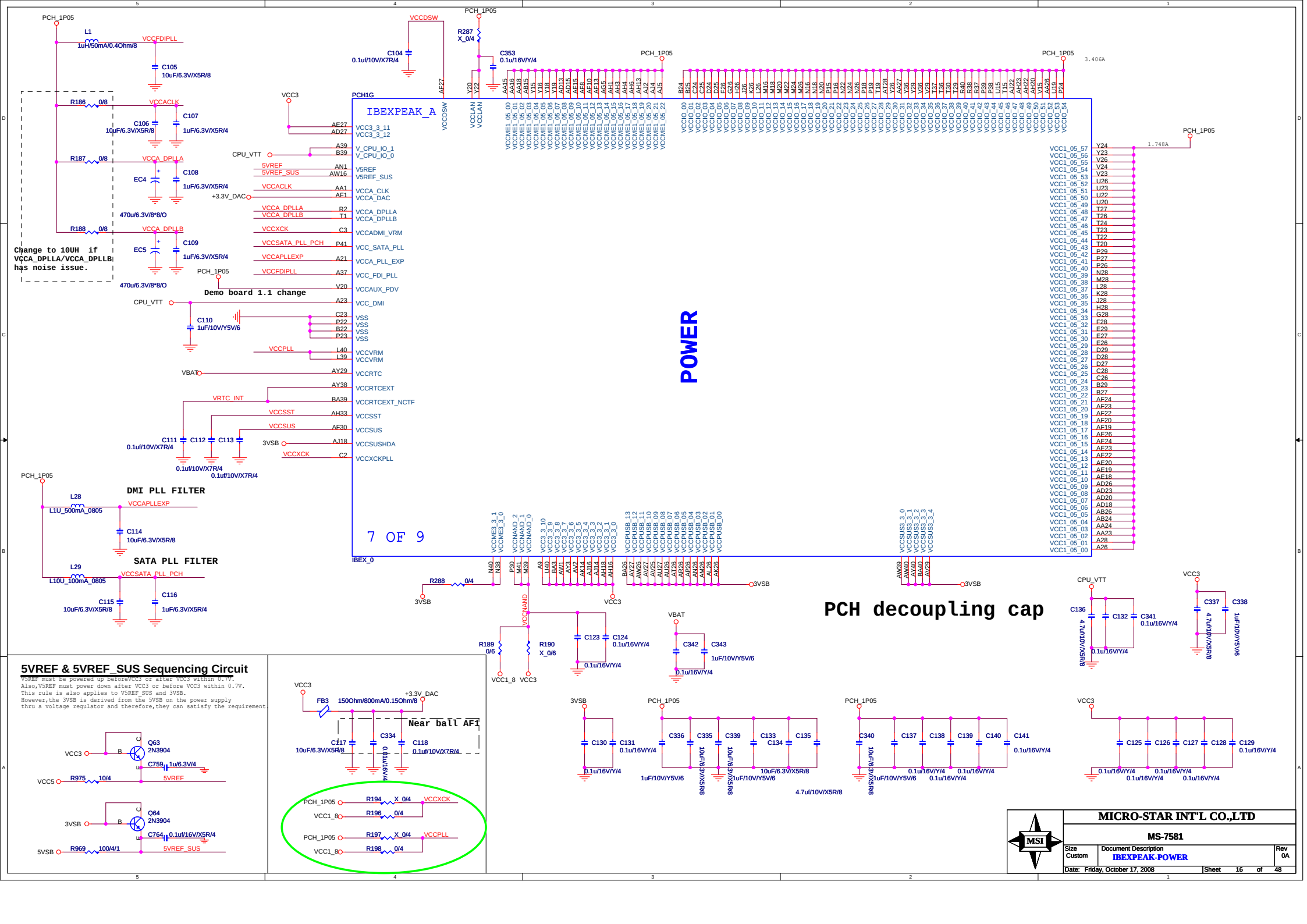


		PCH JTAG Enable		PCH JTAG Disable	
PCH Pin	RefDes	ES1	ES2	ES1	ES2
TDO	R1	No Stff	200 OHM	No Stff	No Stff
	R2	No Stff	100 OHM	No Stff	No Stff
TMS	R3	200 OHM	200 OHM	No Stff	No Stff
	R4	100 OHM	100 OHM	No Stff	No Stff
TDI	R5	200 OHM	200 OHM	20K OHM	No Stff
	R6	100 OHM	100 OHM	10K OHM	No Stff
TCK	R7	51 OHM	51 OHM	51 OHM	51 OHM
TRST#	R8	20K OHM	20K OHM	No Stff	No Stff
	R9	10K OHM	10K OHM	No Stff	No Stff


POWER
PCH decoupling cap
IBEXPEAK_A
PCH1G
7 OF 9
IBEX_0
Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
Demo board 1.1 change
DMI PLL FILTER
SATA PLL FILTER
Near ball AF1
5VREF & 5VREF_SUS Sequencing Circuit
V5REF must be powered up beforeVCC3 or after VCC3 within 0.7V.
Also,V5REF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to V5REF_SUS and 3VSB.
However,the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore,they can satisfy the requirement.
MICRO-STAR INT'L CO.,LTD
MS-7581
IBEXPEAK-POWER
Date: Friday, October 17, 2008
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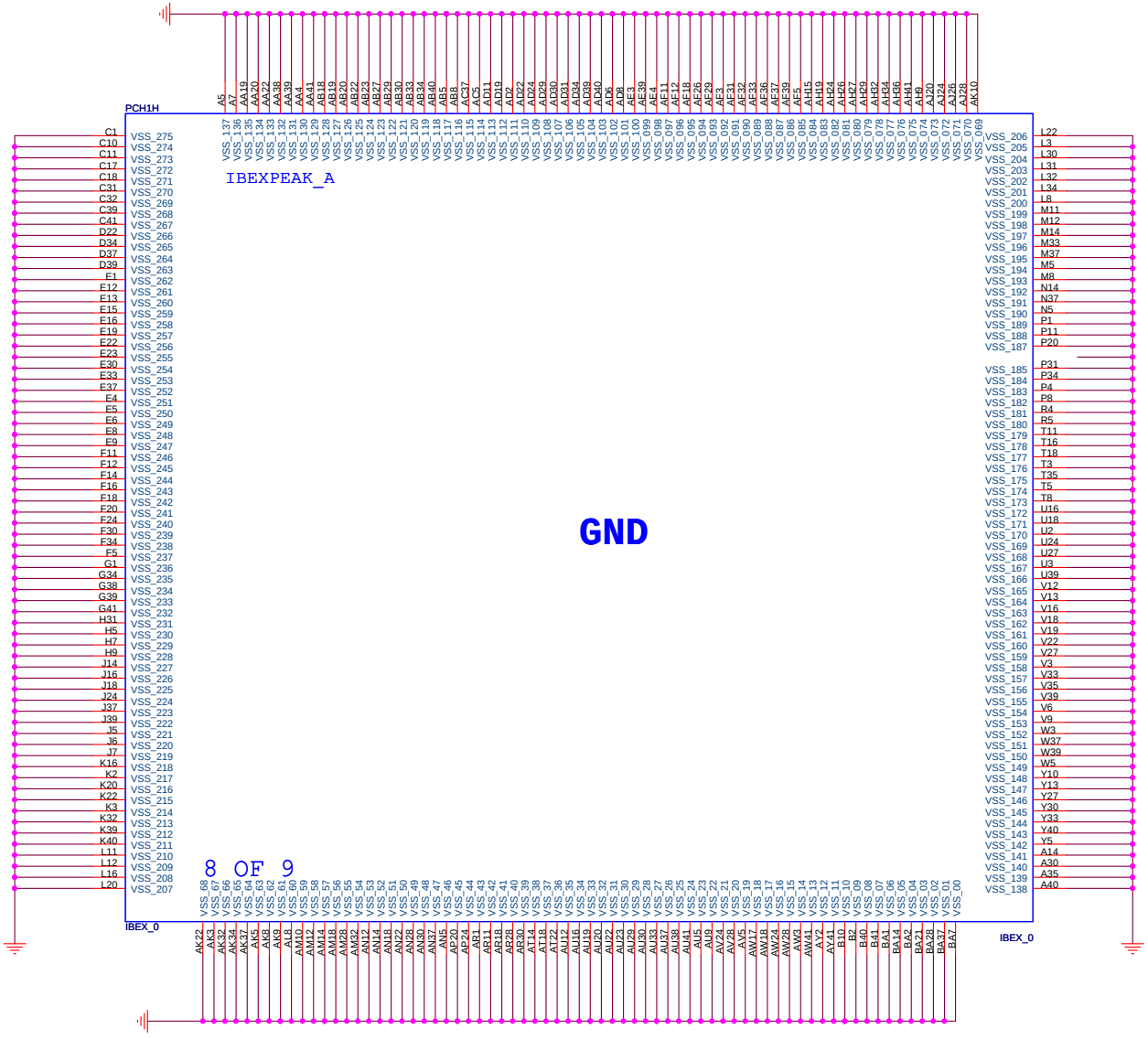

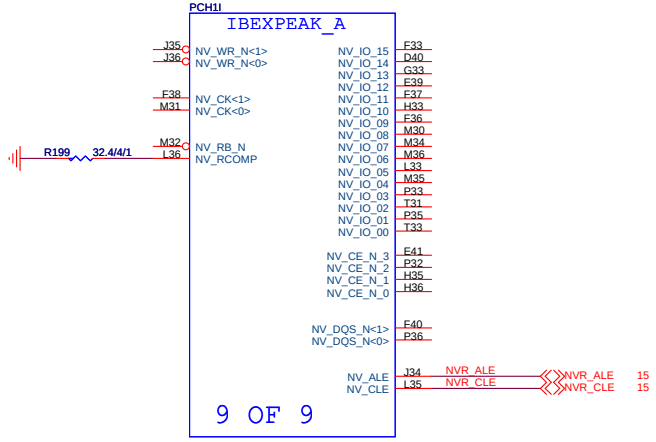

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MS-7581		
Size: Custom	Document Description: IBEXPEAK-GND/NVRAM	Rev: 0A
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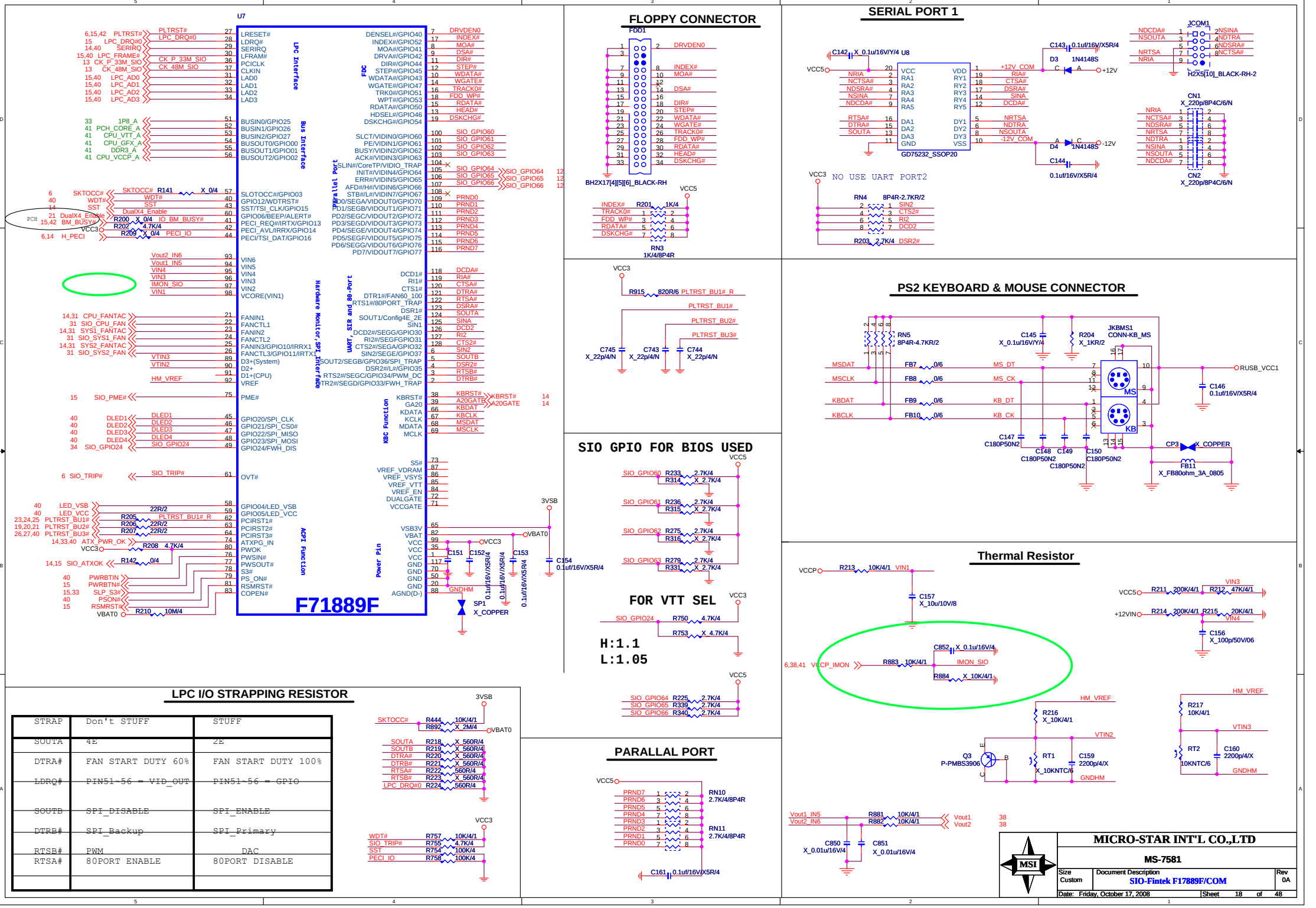
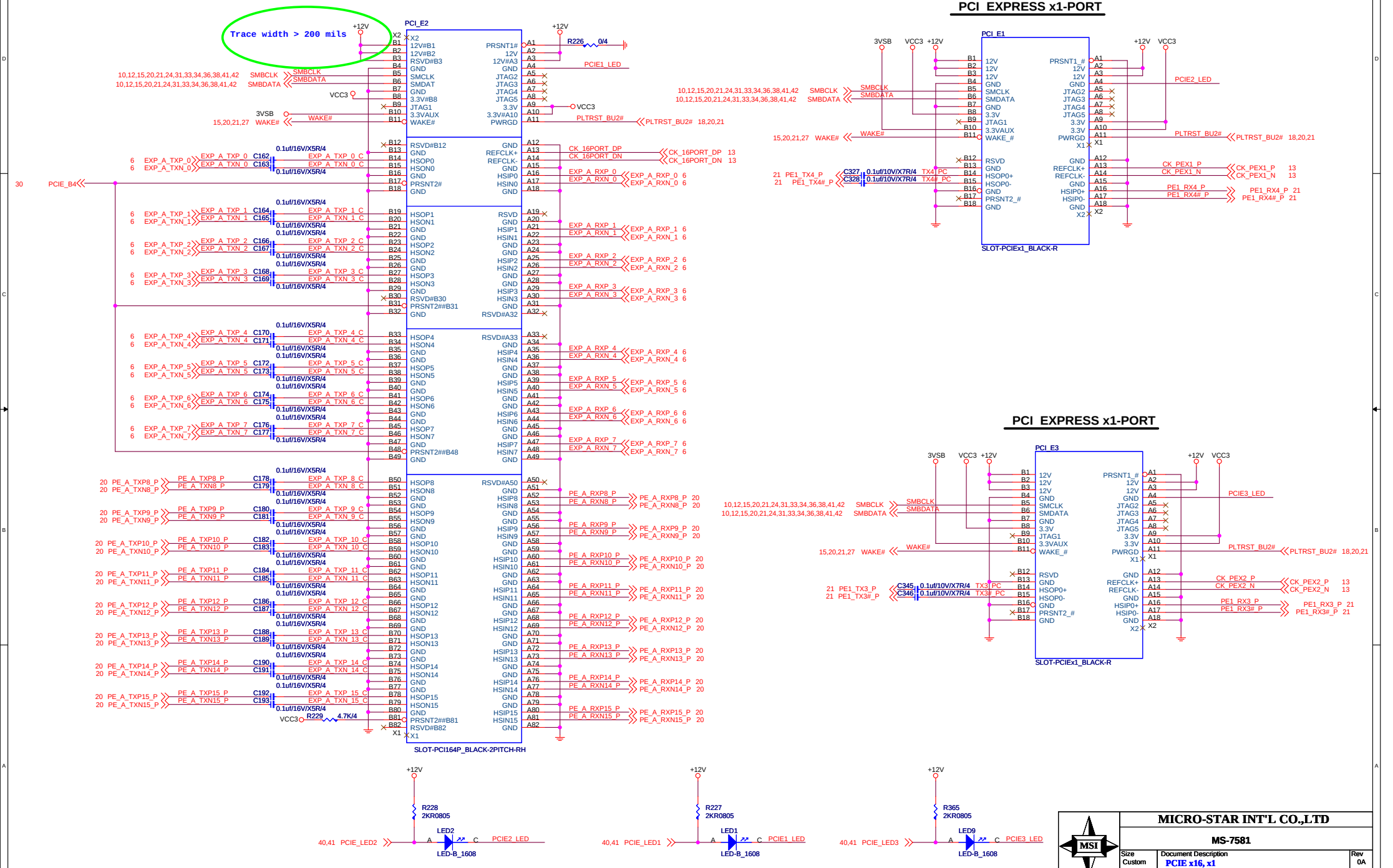


LPC I/O STRAPPING RESISTOR

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51~56 = VID_OUT	PIN51~56 = GPIO
SOUTB	SPI_DISABLE	SPI_ENABLE
DTRB#	SPI_Backup	SPI_Primary
RTSB#	PWM	DAC
RTSA#	80PORT ENABLE	80PORT DISABLE

PCI_Express X16 Slot



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MS-7581	
Size: Custom	Document Description: PCIE x16, x1
Rev: 0A	
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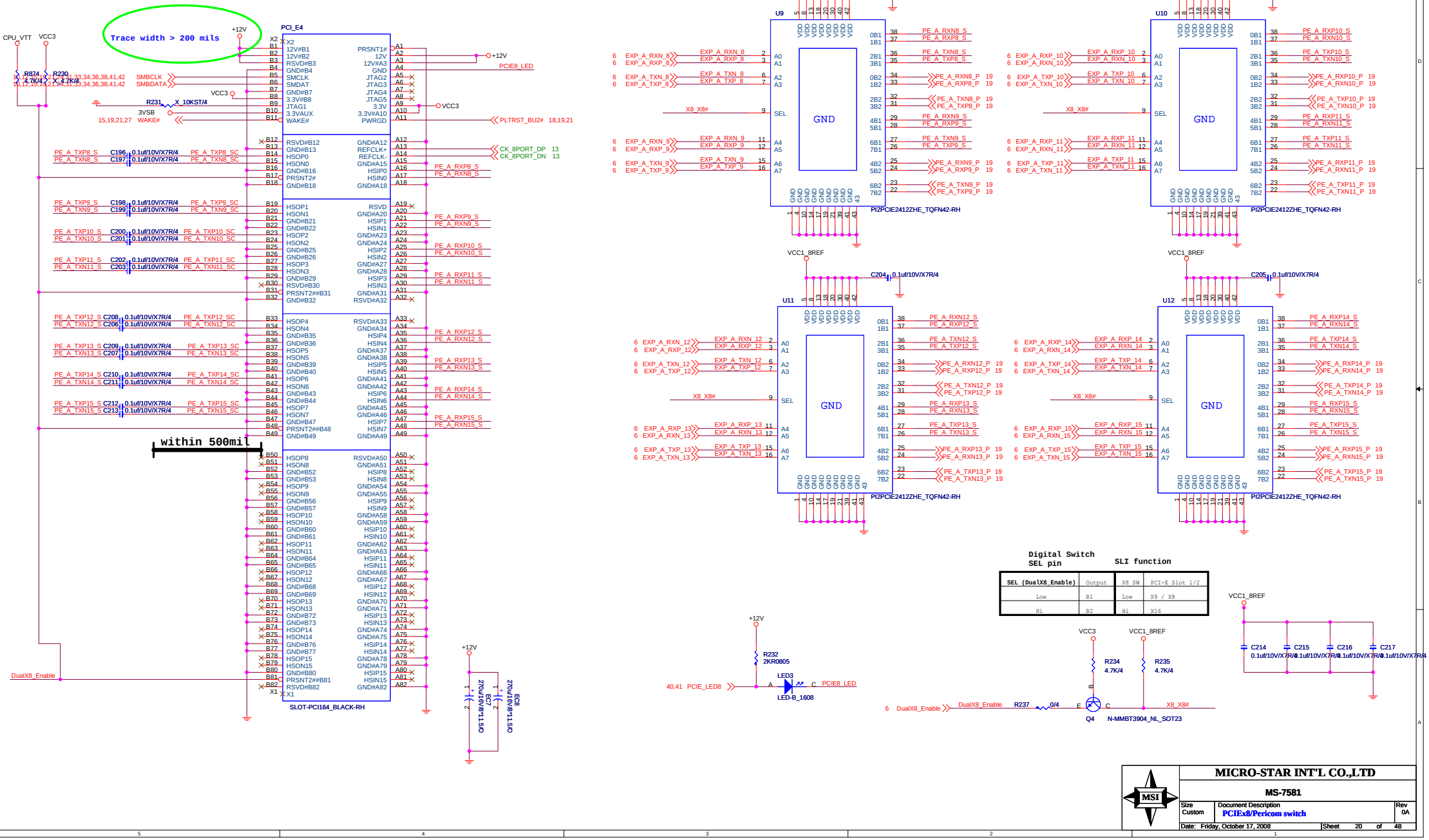
PCI_Express X8 Slot
(Share with PCI_E x16 Slots)



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7581	
Size: Custom	Document Description: PCIEx8/Pericom switch	Rev: 0A
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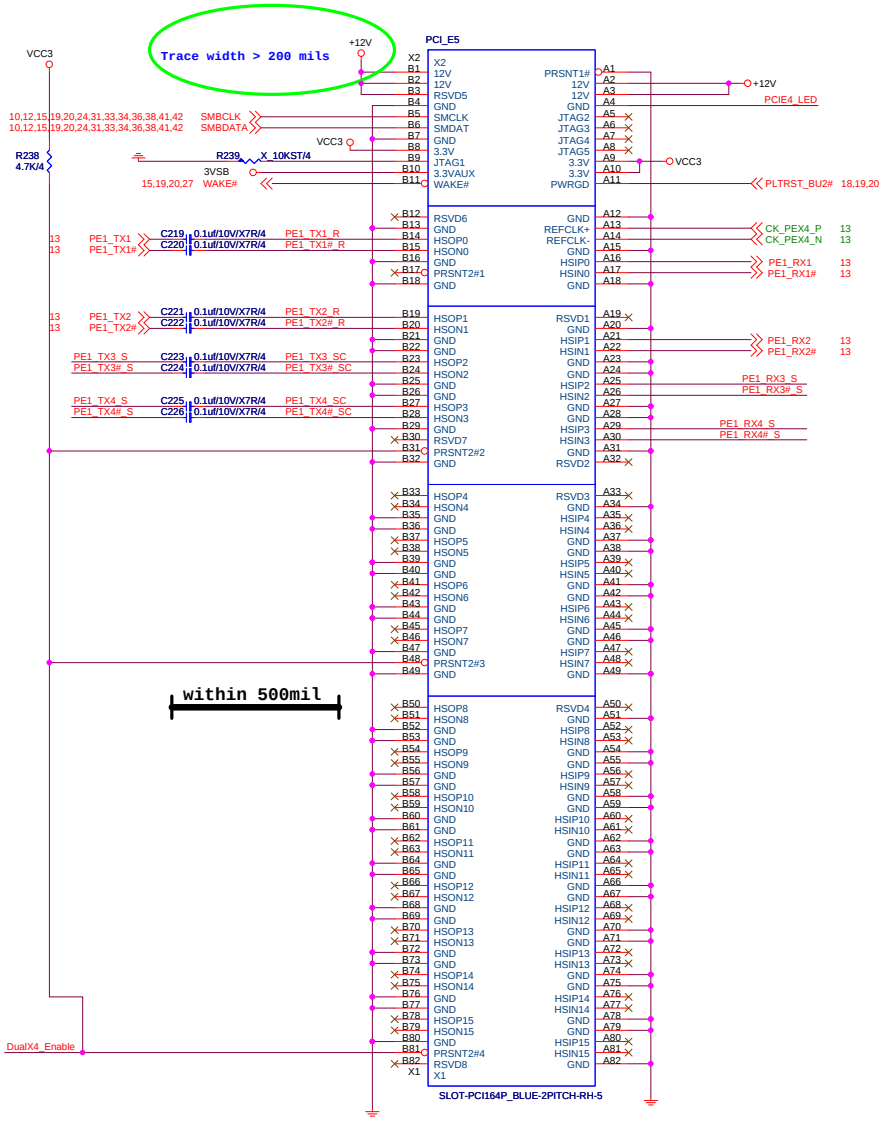
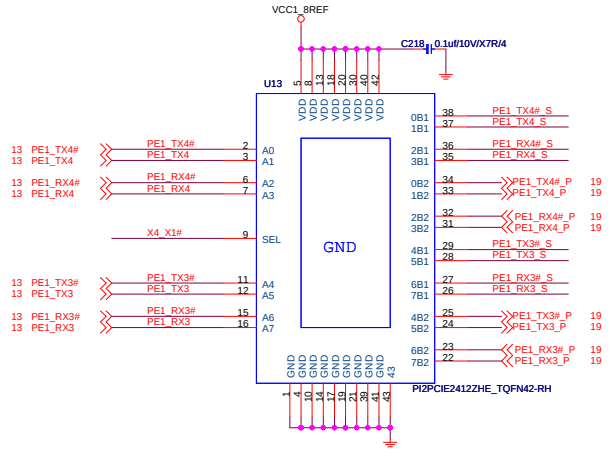
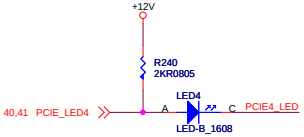
PCI_Express X4 Slot
(Share with PCI_E x1 Slots)

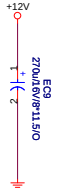


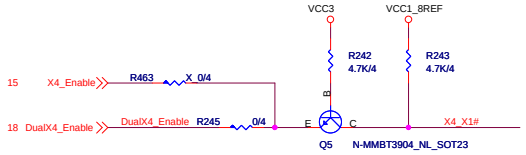


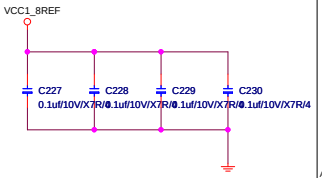
Digital Switch
SEL pin **SLI function**

SEL (DualX8_Enable)	Output	X4_SW	PCI-E Slot 1/2
Low	B1	Low	X4
Hi	B2	Hi	X1 / X1









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MS-7581	
Size: Custom	Document Description: PCIEx8/Pericom switch
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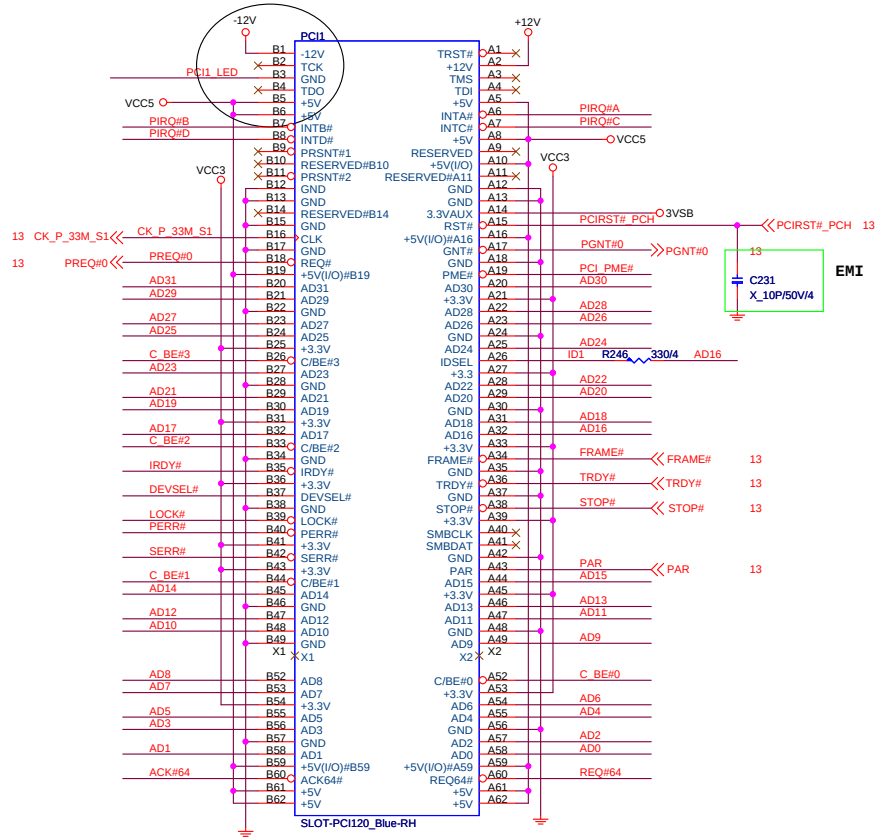
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

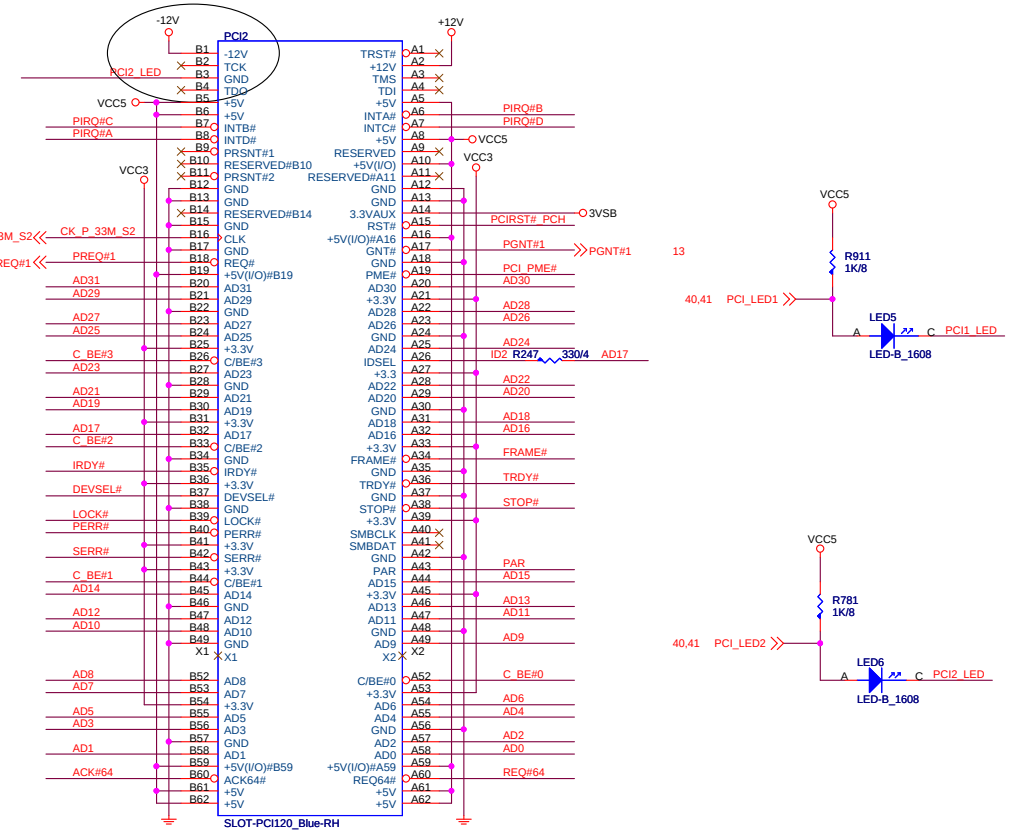


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

13 AD[31..0] — AD[31..0]

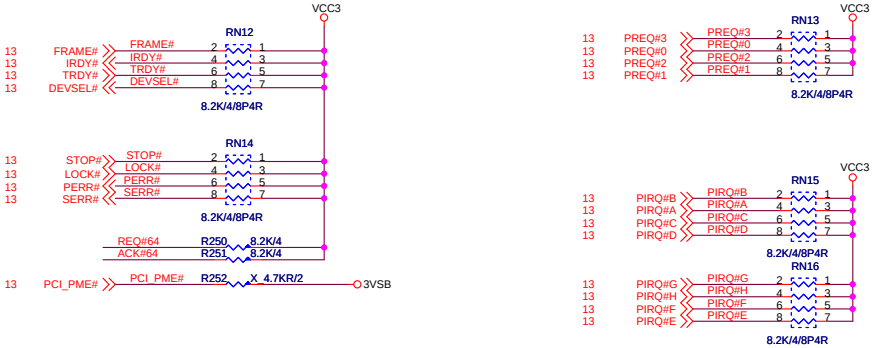
13 C_BE#[3..0] — C_BE#[3..0]

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

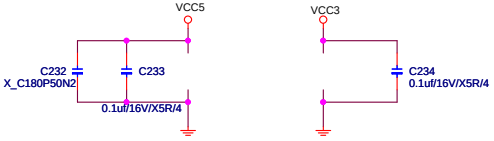


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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Size: Custom	Document Description: PCI Slot 1 & 2	Rev: 0A
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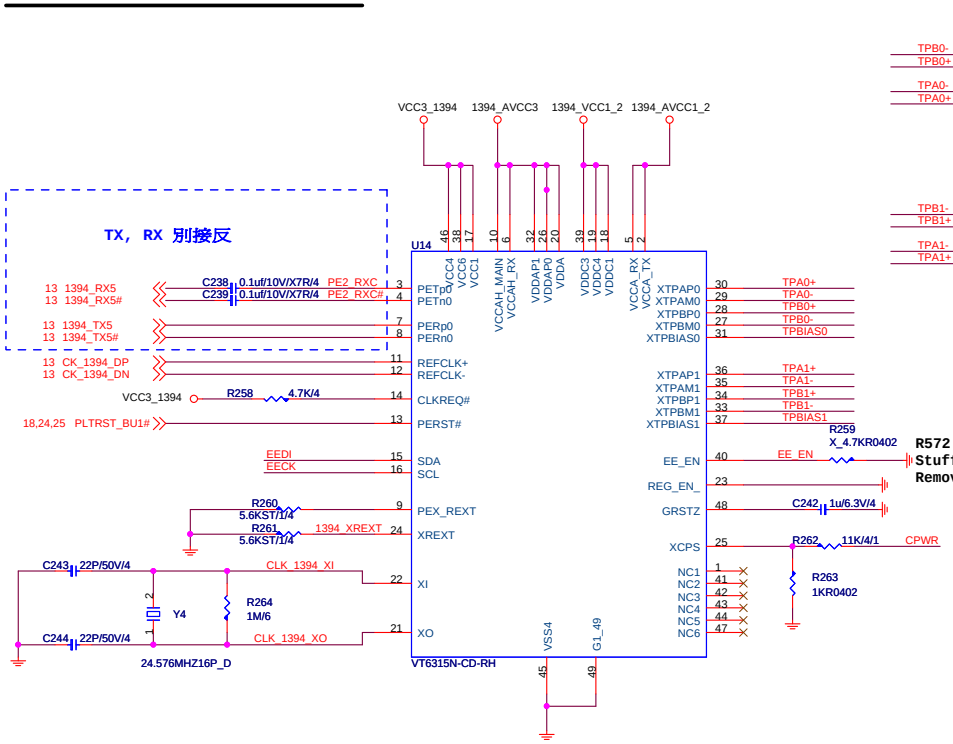
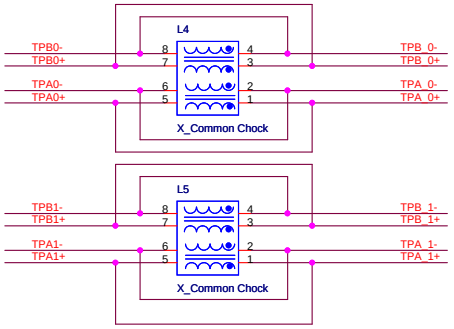
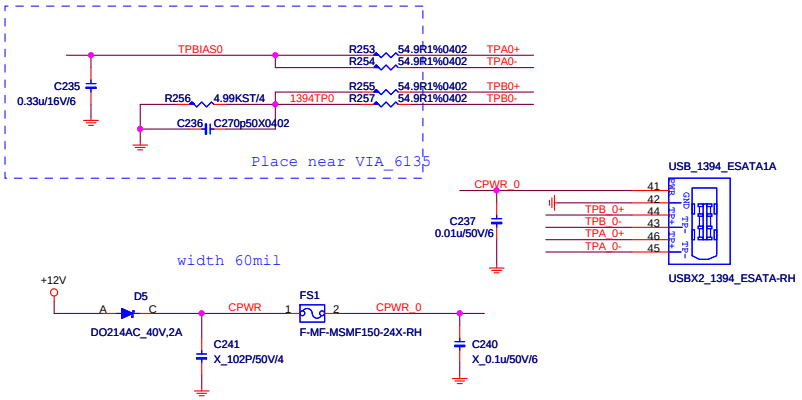
1394 CONTROLLER



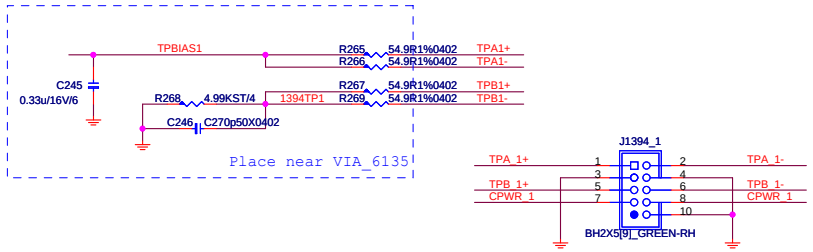
R572 :
Stuff:disable EE PROM
Remove:enable EE PROM

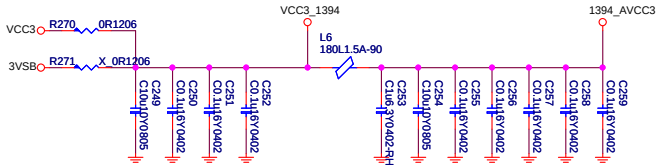


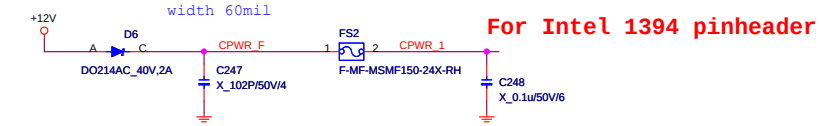
Rear 1394 port



Front 1394 pin header

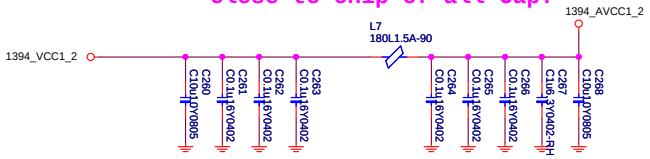




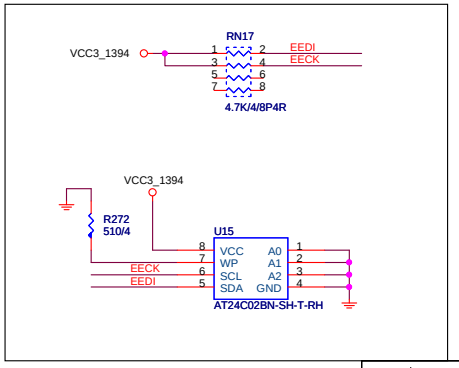


For Intel 1394 pinheader

close to chip of all Cap.



close to chip of all Cap.



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MS-7581		
Size: Custom	Document Description: 1394 Controller - VT6315N-CD	Rev: 0A
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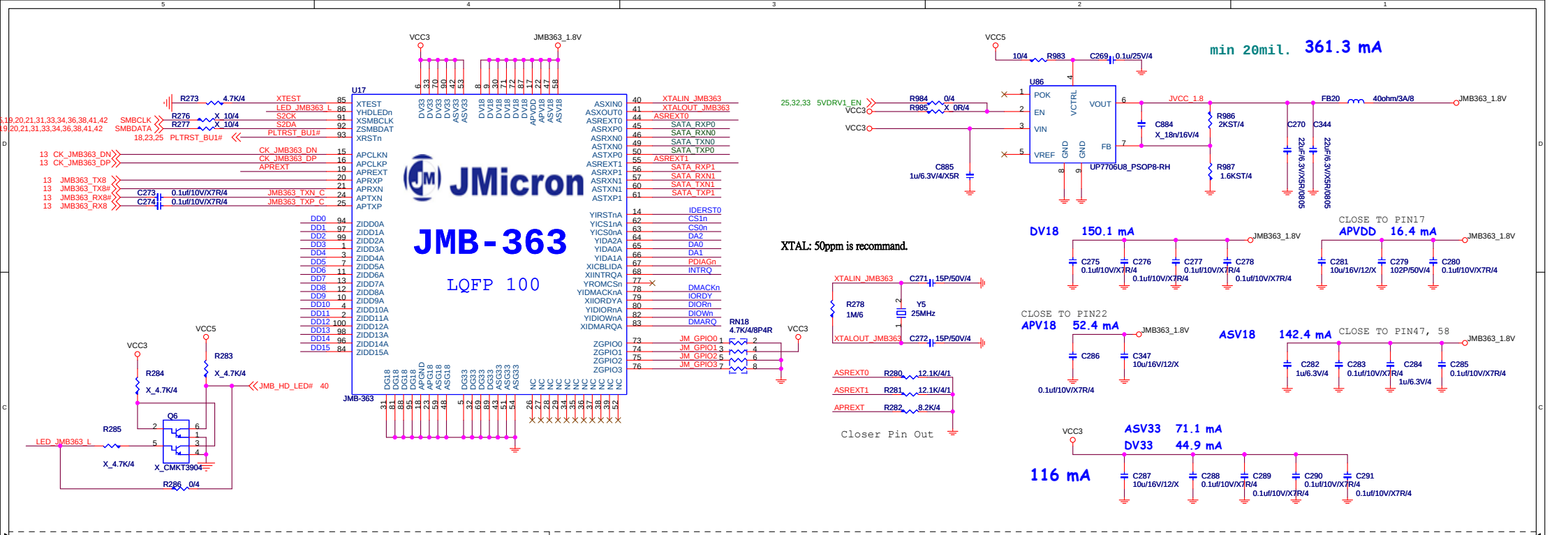
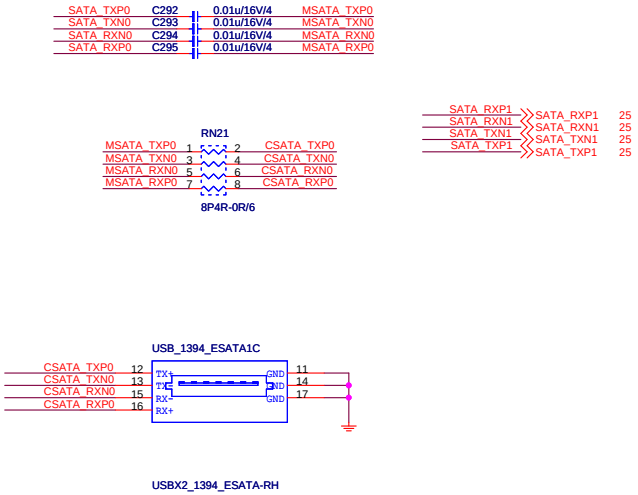
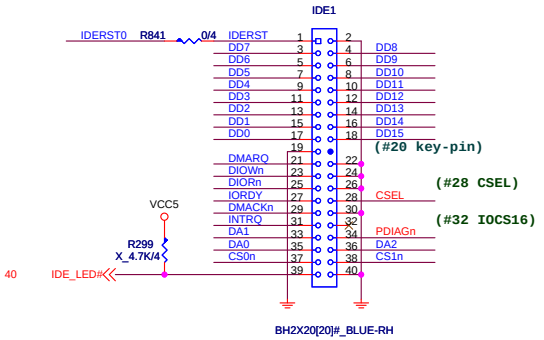


2S



1P



if the length of JMB-363 to IDE connector more than 4inch, that must stuff dampping resistor.

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: JMB-363 E-SATA X1/SATA/ IDE X1	Rev: 0A
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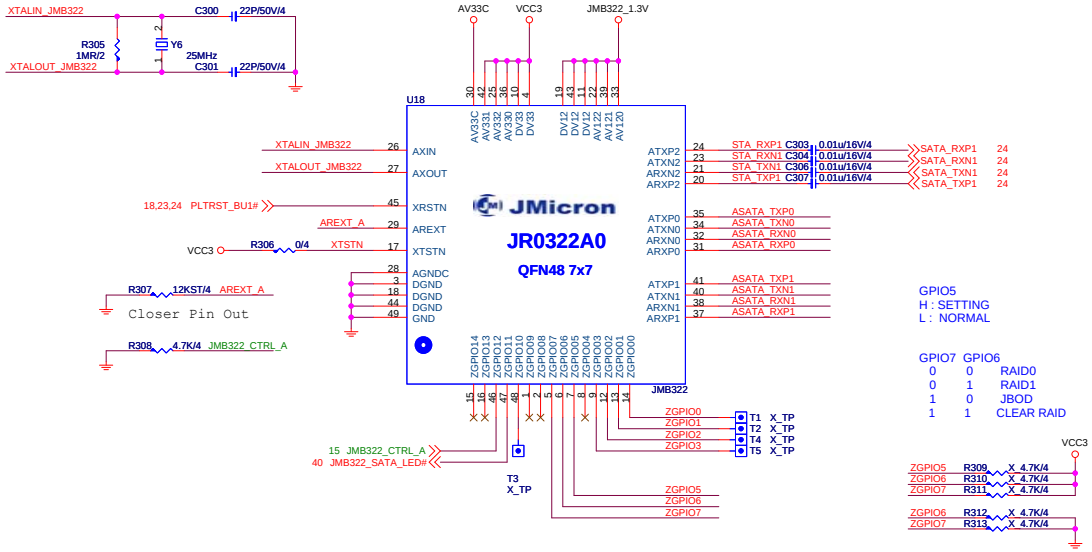
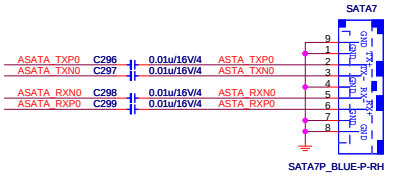
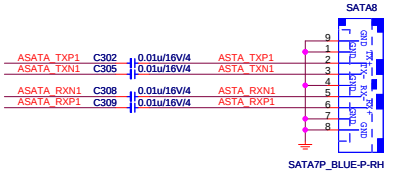
JMB322 - H/W RAID CONTROLLER A

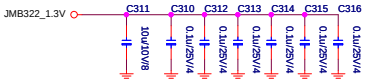


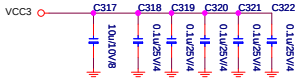
GPIO5
H : SETTING
L : NORMAL

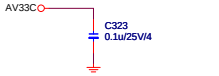
GPIO7	GPIO6	
0	0	RAID0
0	1	RAID1
1	0	JBOD
1	1	CLEAR RAID



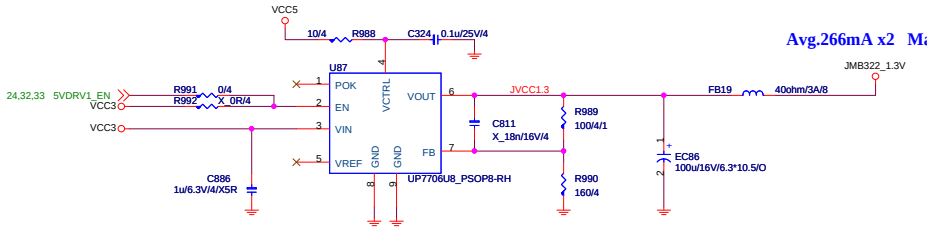








Avg.266mA x2 Max.400mA x2



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MS-7581		
Size: Custom	Document Description: JMB362 PCIE to PATA/SATA	Rev: 0A
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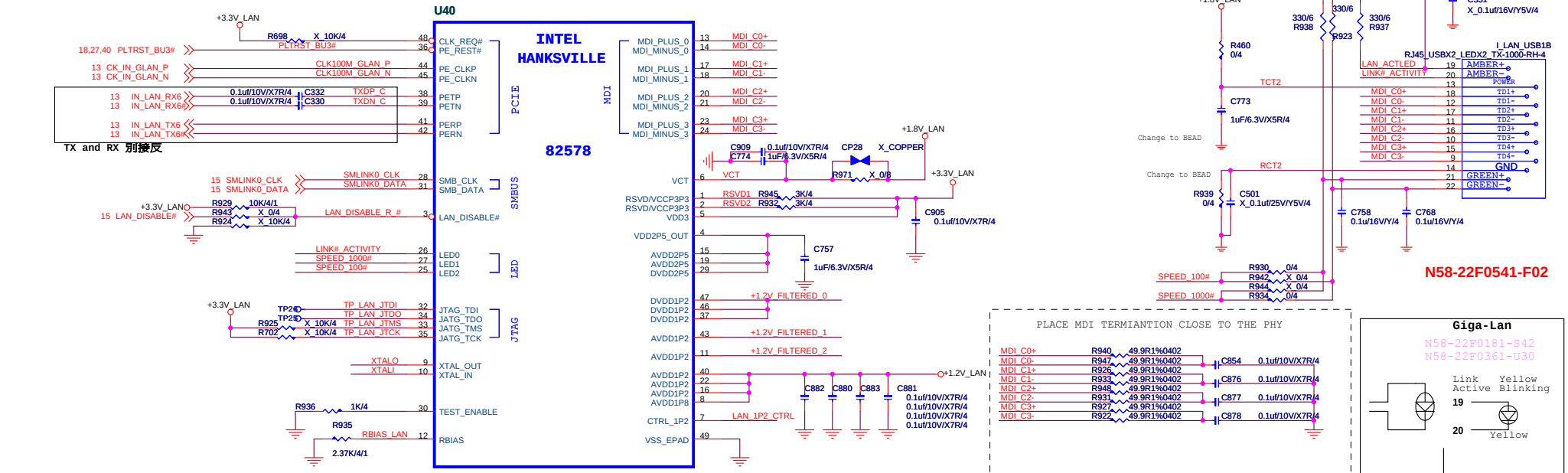
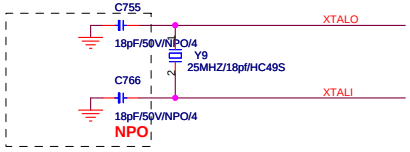
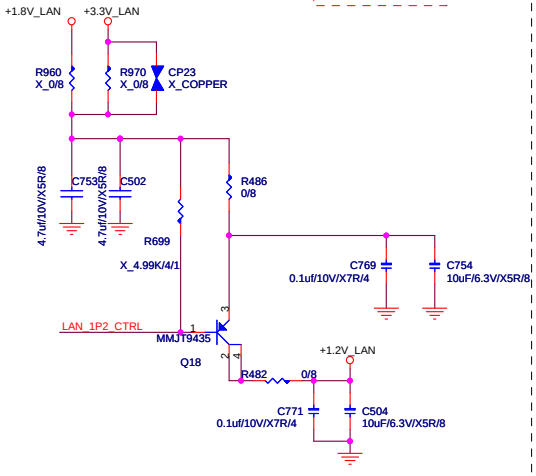
Vo = Vref (1+R2/R1) + ladj x R2



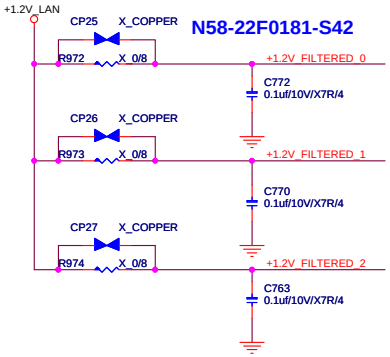


+1.2V_LAN

MMJT9435 Id=3A
BCP69 Id=1A

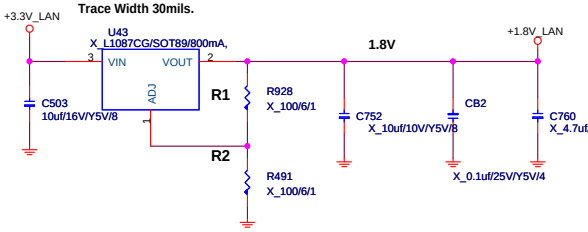


+1.2V_FILTERED 0,1,2

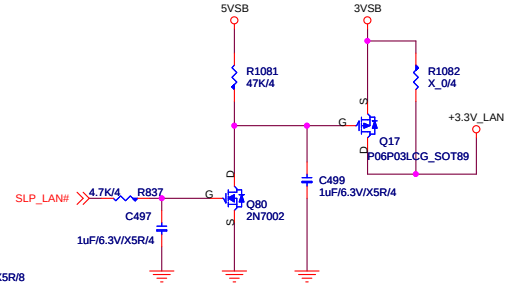


+1.8V_LAN

PN:I31-0108759-N03



+3.3V_LAN



1.PCH Change net name
2. 10 KΩ pull-up resistor at the SLP_LAN# output of the PCH
3.reserve a 0 ohm between RSM_RST and LAN_RST

MICRO-STAR INT'L CO.,LTD		
MS-7581		
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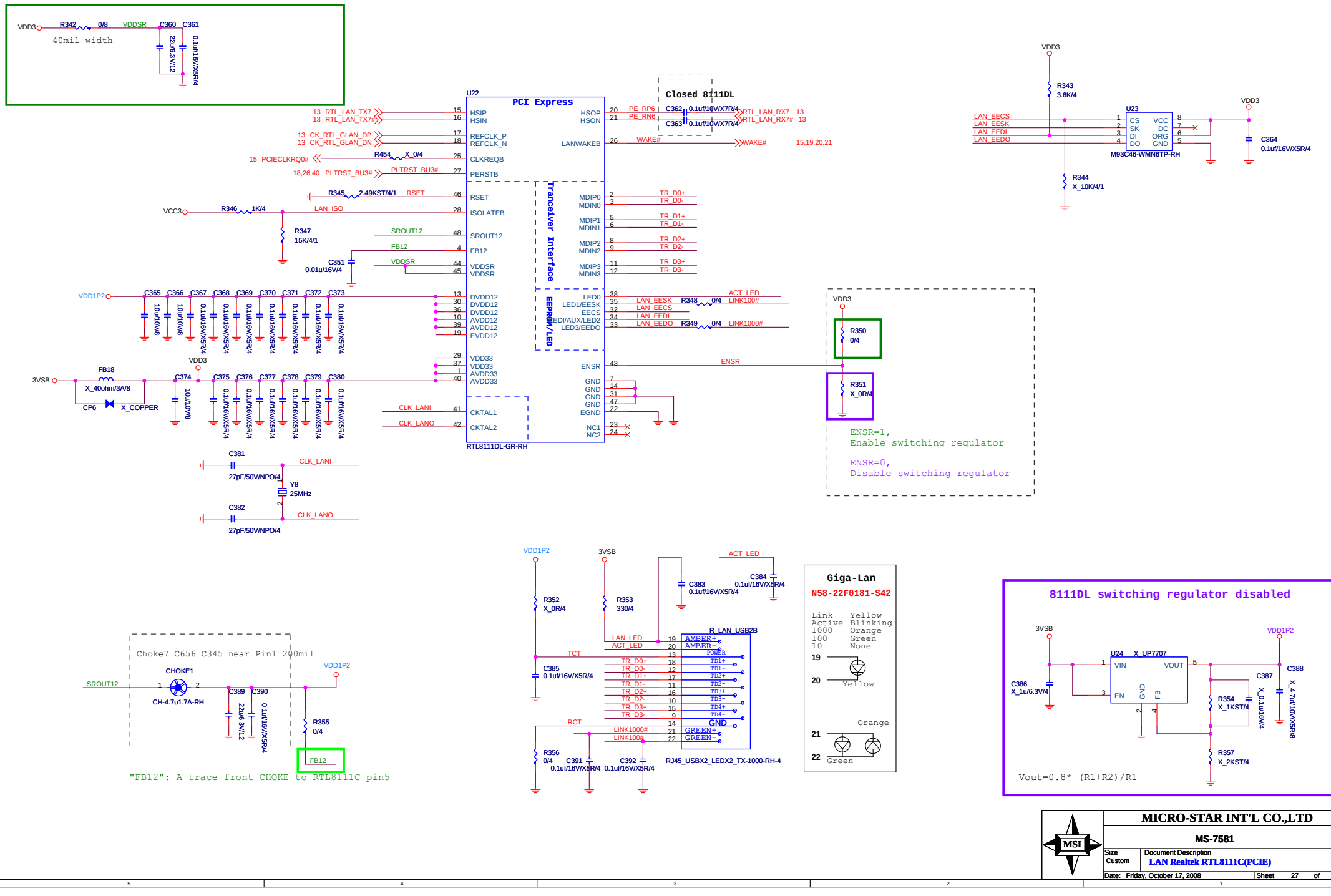

MICRO-STAR INT'L CO.,LTD	
MS-7581	
Size: Custom	Document Description: LAN Realtek RTL8111C(PCIE)
Rev: 0A	
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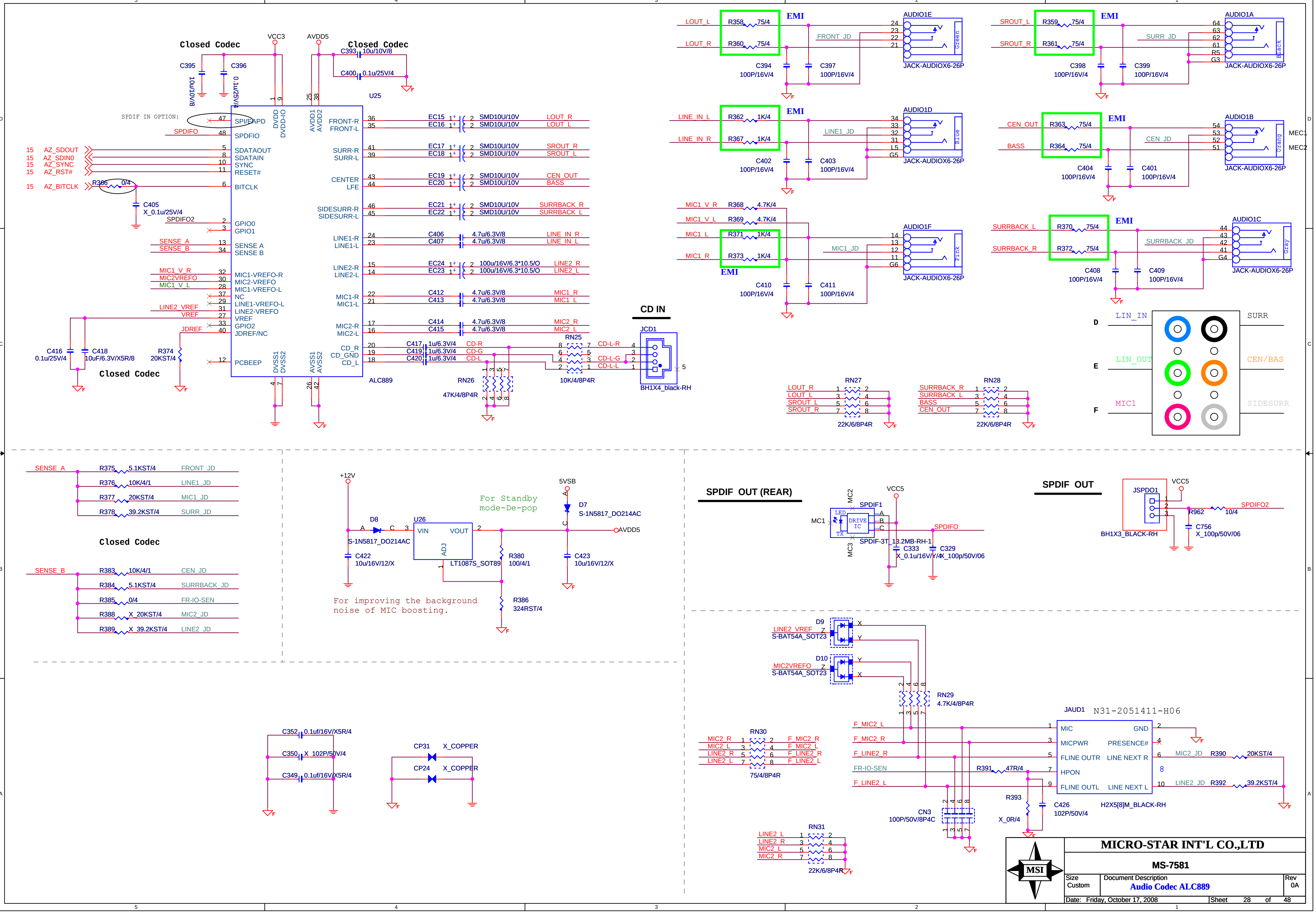
Closed Codec
VCC3
AVDD5
Closed Codec
C393 10u/10V/8
C400 0.1u/25V/4
C395
C396
10u/10V/8
0.1u/25V/4
U25
SPDIF IN OPTION:
SPDIFO
15 AZ_SDOUT
15 AZ_SDIN0
15 AZ_SYNC
15 AZ_RST#
15 AZ_BITCLK
R366 0/4
C405
X_0.1u/25V/4
SPDIFO2
SENSE_A
SENSE_B
MIC1_V_R
MIC2VREFO
MIC1_V_L
LINE2_VREF
VREF
JDREF
SPI/EAPD
SPDFIO
SDATAOUT
SDATAIN
SYNC
RESET#
BITCLK
GPIO0
GPIO1
SENSE A
SENSE B
MIC1-VREFO-R
MIC2-VREFO
MIC1-VREFO-L
NC
LINE1-VREFO-L
LINE2-VREFO
VREF
GPIO2
JDREF/NC
PCBEEP
DVDD
DVDD-IO
AVDD1
AVDD2
DVSS1
DVSS2
AVSS1
AVSS2
FRONT-R
FRONT-L
SURR-R
SURR-L
CENTER
LFE
SIDESURR-R
SIDESURR-L
LINE1-R
LINE1-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
MIC2-R
MIC2-L
CD_R
CD_GND
CD_L
ALC889
C416 0.1u/25V/4
C418 10uF/6.3V/X5R/8
R374 20KST/4
Closed Codec
EC15 SMD10U/10V LOUT_R
EC16 SMD10U/10V LOUT_L
EC17 SMD10U/10V SROUT_R
EC18 SMD10U/10V SROUT_L
EC19 SMD10U/10V CEN_OUT
EC20 SMD10U/10V BASS
EC21 SMD10U/10V SURRBACK_R
EC22 SMD10U/10V SURRBACK_L
C406 4.7u/6.3V/8 LINE_IN_R
C407 4.7u/6.3V/8 LINE_IN_L
EC24 100u/16V/6.3*10.5/O LINE2_R
EC23 100u/16V/6.3*10.5/O LINE2_L
C412 4.7u/6.3V/8 MIC1_R
C413 4.7u/6.3V/8 MIC1_L
C414 4.7u/6.3V/8 MIC2_R
C415 4.7u/6.3V/8 MIC2_L
C417 1u/6.3V/4 CD-R
C419 1u/6.3V/4 CD-G
C420 1u/6.3V/4 CD-L
RN26 47K/4/8P4R
RN25 10K/4/8P4R
CD-L-R
CD-L-G
CD-L-L
CD IN
JCD1
BH1X4_black-RH
LOUT_L
LOUT_R
R358 75/4
R360 75/4
EMI
FRONT_JD
C394 100P/16V/4
C397 100P/16V/4
AUDIO1E
JACK-AUDIOX6-26P
Green
SROUT_L
SROUT_R
R359 75/4
R361 75/4
SURR_JD
C398 100P/16V/4
C399 100P/16V/4
AUDIO1A
Black
LINE_IN_L
LINE_IN_R
R362 1K/4
R367 1K/4
LINE1_JD
C402 100P/16V/4
C403 100P/16V/4
AUDIO1D
Blue
CEN_OUT
BASS
R363 75/4
R364 75/4
CEN_JD
C404 100P/16V/4
C401 100P/16V/4
AUDIO1B
Orang
MEC1
MEC2
MIC1_V_R R368 4.7K/4
MIC1_V_L R369 4.7K/4
MIC1_L R371 1K/4
MIC1_R R373 1K/4
MIC1_JD
C410 100P/16V/4
C411 100P/16V/4
AUDIO1F
Pink
SURRBACK_L
SURRBACK_R
R370 75/4
R372 75/4
SURRBACK_JD
C408 100P/16V/4
C409 100P/16V/4
AUDIO1C
Gray
LIN_IN
SURR
LIN_OUT
CEN/BAS
MIC1
SIDESURR
RN27 22K/6/8P4R
RN28 22K/6/8P4R
SENSE_A R375 5.1KST/4 FRONT_JD
R376 10K/4/1 LINE1_JD
R377 20KST/4 MIC1_JD
R378 39.2KST/4 SURR_JD
Closed Codec
SENSE_B R383 10K/4/1 CEN_JD
R384 5.1KST/4 SURRBACK_JD
R385 0/4 FR-IO-SEN
R388 X_20KST/4 MIC2_JD
R389 X_39.2KST/4 LINE2_JD
+12V
D8
S-1N5817_DO214AC
C422 10u/16V/12/X
U26
VIN VOUT ADJ
LT1087S_SOT89
R380 100/4/1
R386 324RST/4
5VSB
D7
S-1N5817_DO214AC
AVDD5
C423 10u/16V/12/X
For Standby
mode-De-pop
For improving the background
noise of MIC boosting.
SPDIF OUT (REAR)
SPDIF1
VCC5
MC1
MC2
MC3
LED
DRIVE IC
SPDIF-3T_13.2MB-RH-1
SPDIFO
C333 X_0.1u/16V/Y/4
C329 X_100p/50V/06
SPDIF OUT
JSPDO1
VCC5
R962 10/4
SPDIFO2
C756 X_100p/50V/06
BH1X3_BLACK-RH
D9 S-BAT54A_SOT23
LINE2_VREF
D10 S-BAT54A_SOT23
MIC2VREFO
RN29 4.7K/4/8P4R
JAUD1 N31-2051411-H06
MIC GND
MICPWR PRESENCE#
FLINE OUTR LINE NEXT R
HPON
FLINE OUTL LINE NEXT L
F_MIC2_L
F_MIC2_R
F_LINE2_R
FR-IO-SEN
F_LINE2_L
R391 47R/4
R390 20KST/4 MIC2_JD
R392 39.2KST/4 LINE2_JD
R393 X_0R/4
C426 102P/50V/4
H2X5[8]M_BLACK-RH
CN3 100P/50V/8P4C
RN30 75/4/8P4R
RN31 22K/6/8P4R
C352 0.1uf/16V/X5R/4
C350 X_102P/50V/4
C349 0.1uf/16V/X5R/4
CP31 X_COPPER
CP24 X_COPPER
MSI
MICRO-STAR INT'L CO.,LTD
MS-7581
Size Custom
Document Description
Audio Codec ALC889
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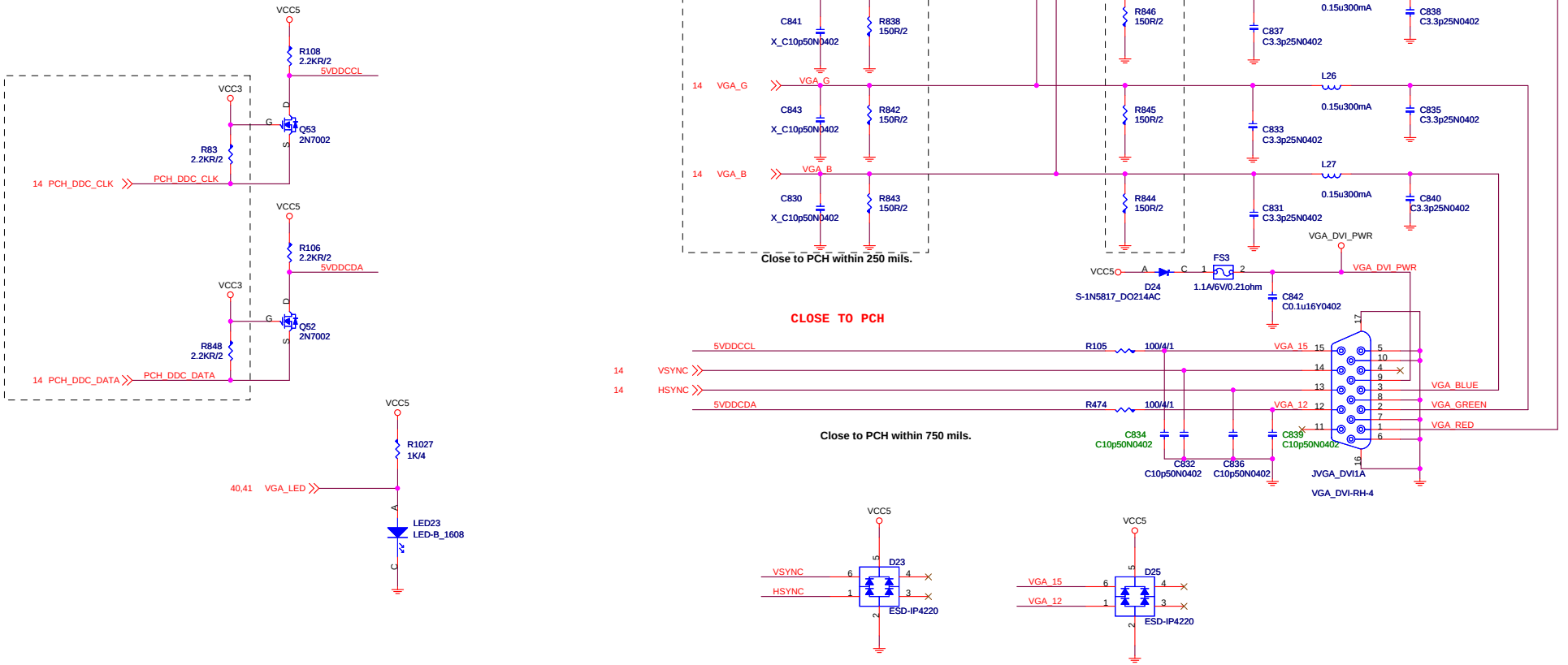
Video Connector



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7581	
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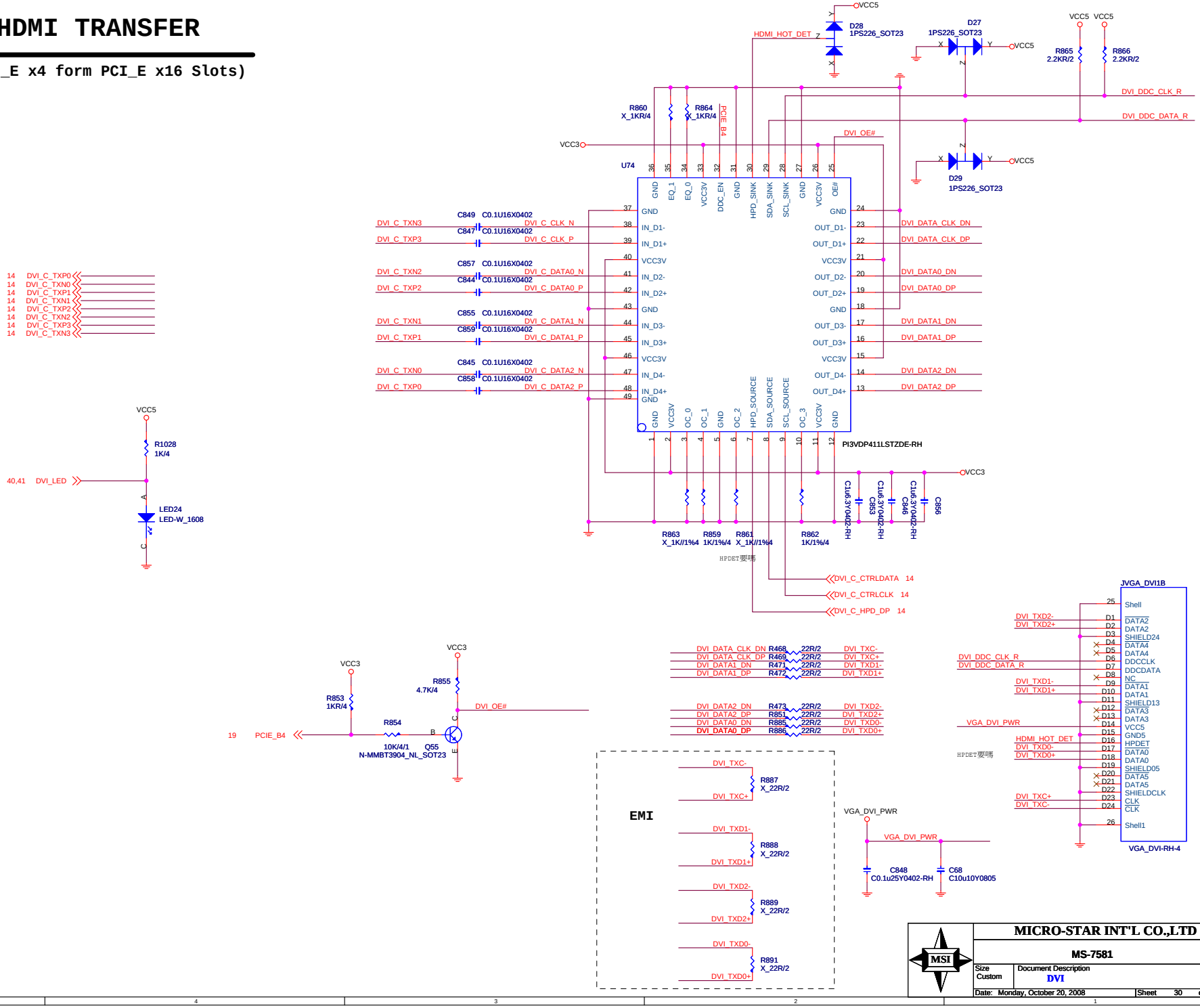
DVI/HDMI TRANSFER

(Share PCI_E x4 form PCI_E x16 Slots)



MICRO-STAR INT'L CO.,LTD		
MS-7581		
Size: Custom	Document Description: DVI	Rev: 0A
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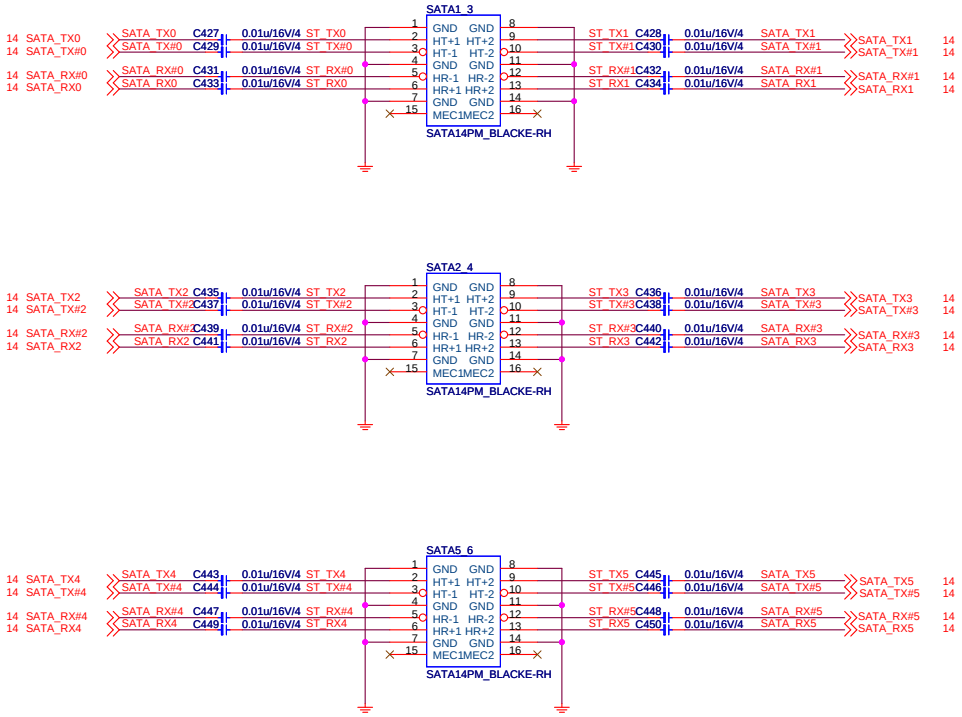
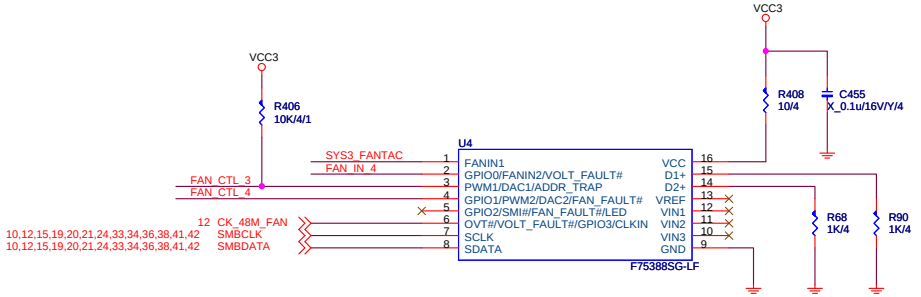


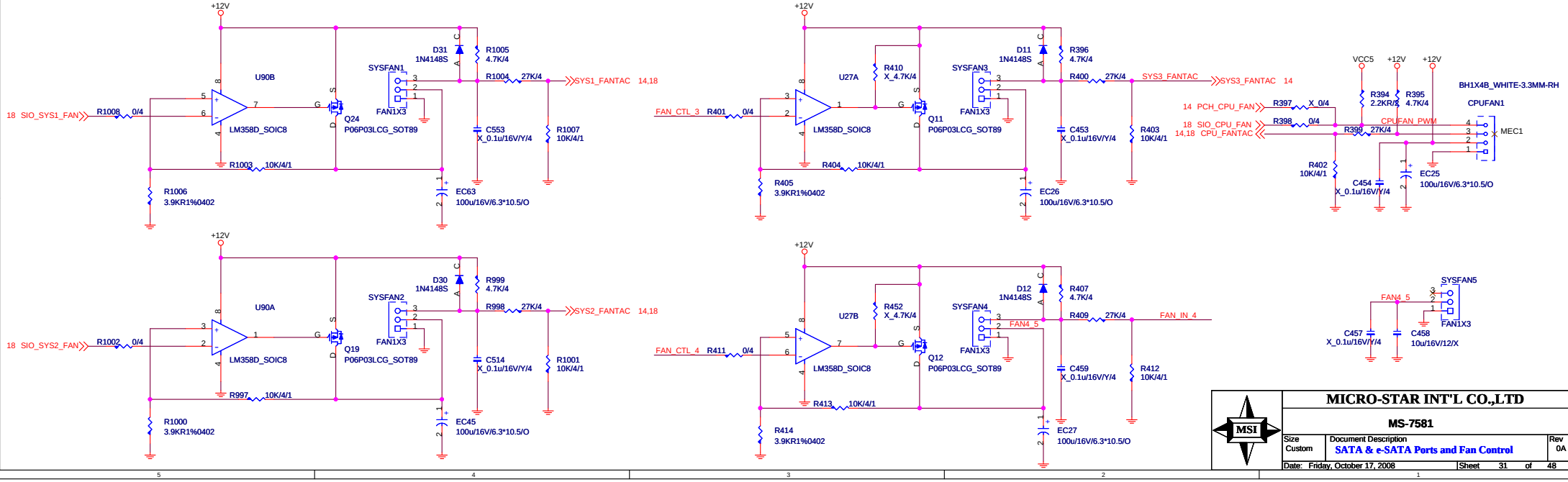
CPU Thermo Sense

FAN initial Speed setting(PIN3)

FAN Speed rate	I2C Address	FAN Type	R89
60%	0x5A	DAC	NC
100%	0x5C	DAC	200K
60%	0x5C	PWM	10K
100%	0x5A	PWM	2.2K



FAN-COUNTROL CIRCUIT



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: SATA & e-SATA Ports and Fan Control
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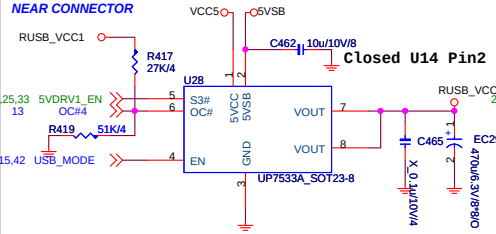
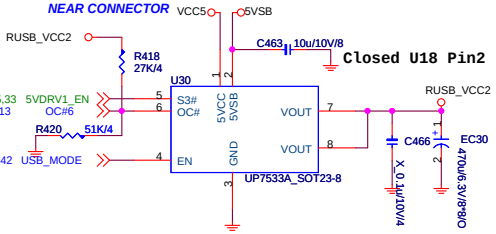
Rear USB Connector

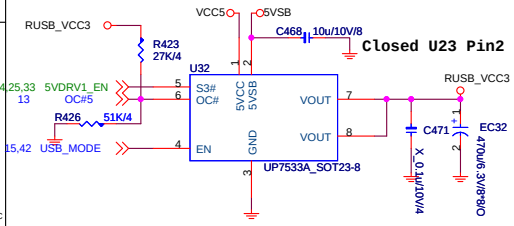
USB POWER FOR PORT 6,7



USB POWER FOR PORT 8,9



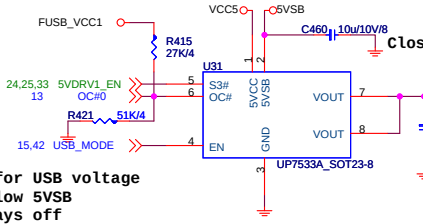
USB POWER FOR PORT 10,11



GPIO for USB voltage
H:Follow 5VSB
L:Always off

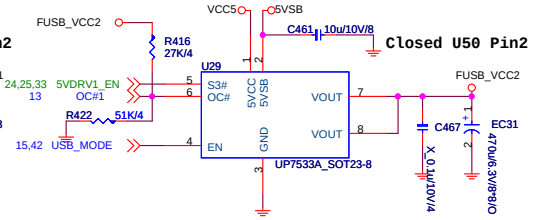
Front USB Connector

USB POWER FOR PORT 0,1

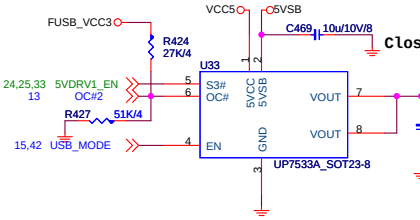


GPIO for USB voltage
H:Follow 5VSB
L:Always off

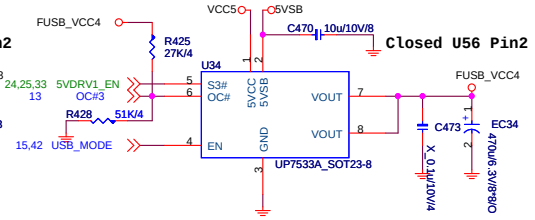
USB POWER FOR PORT 2,3



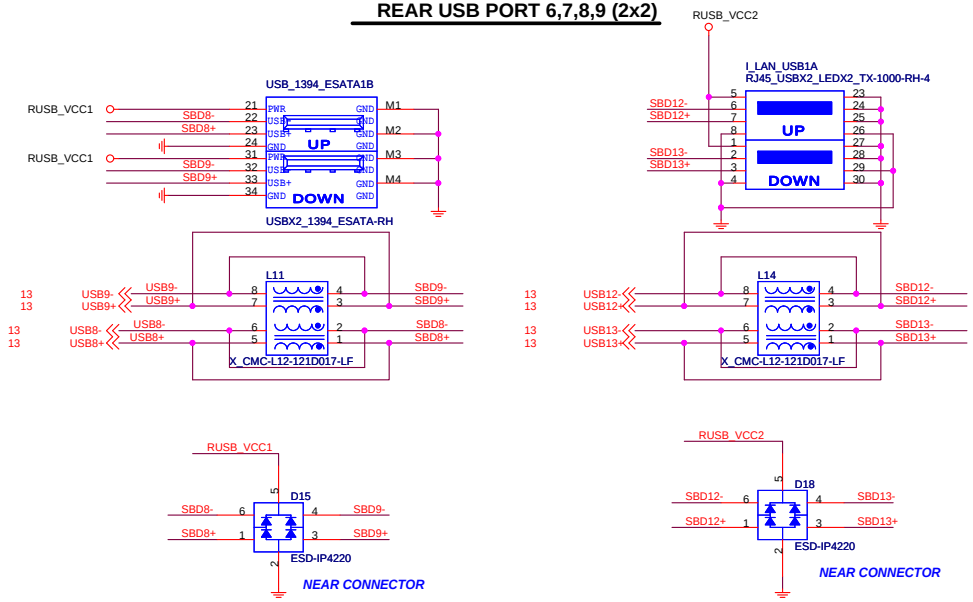
USB POWER FOR PORT 4,5



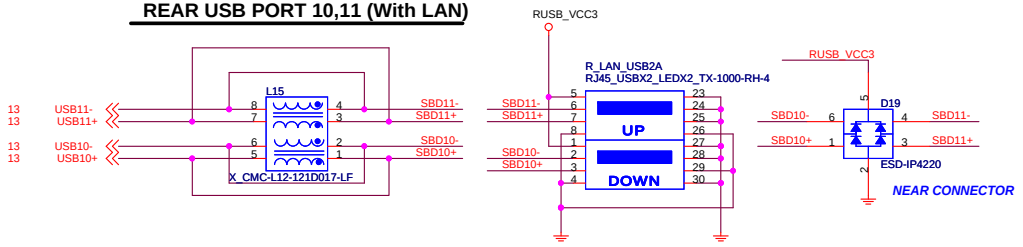
USB POWER FOR PORT 2,3



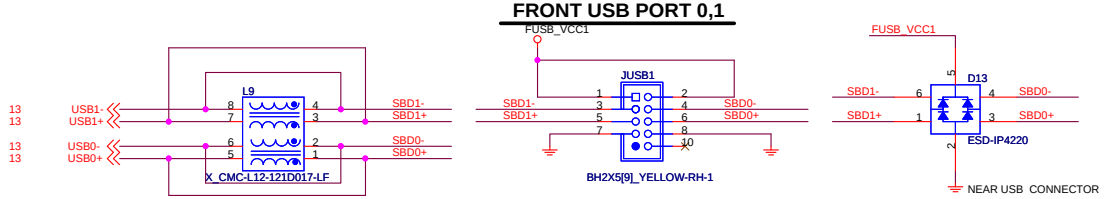
REAR USB PORT 6,7,8,9 (2x2)



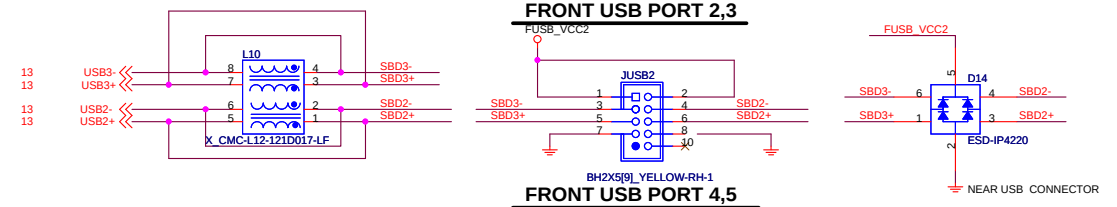
REAR USB PORT 10,11 (With LAN)



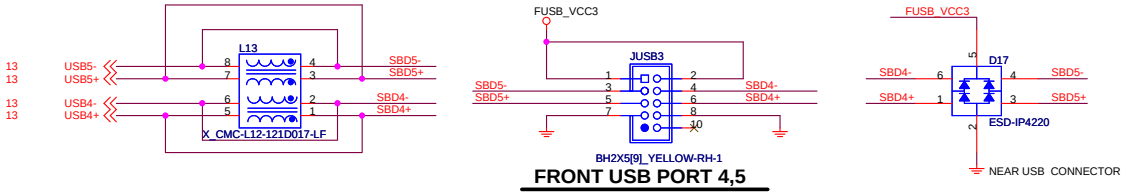
FRONT USB PORT 0,1



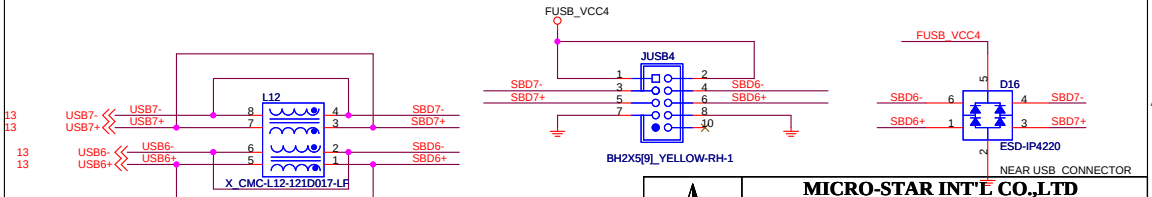
FRONT USB PORT 2,3



FRONT USB PORT 4,5



FRONT USB PORT 4,5



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Custom	USB Connectors-14port	0A

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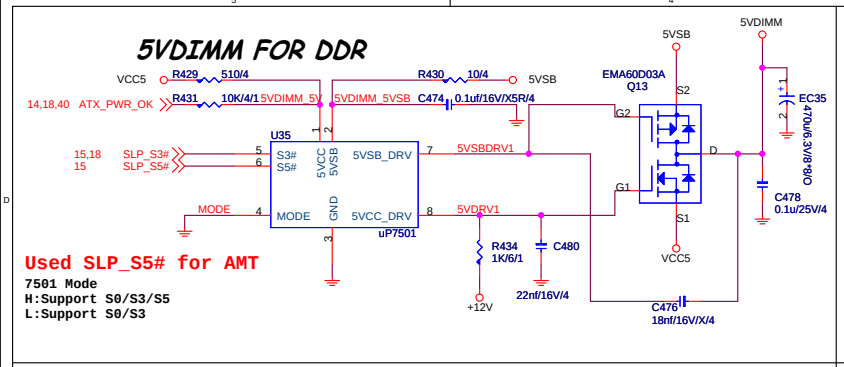

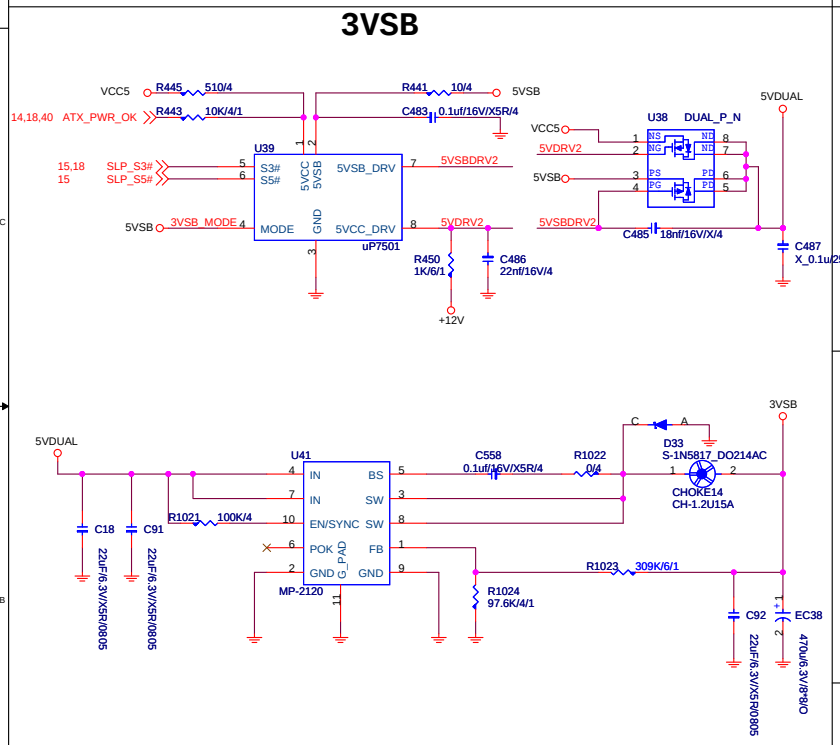

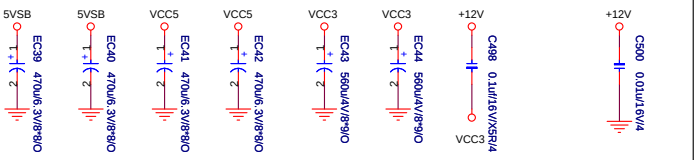

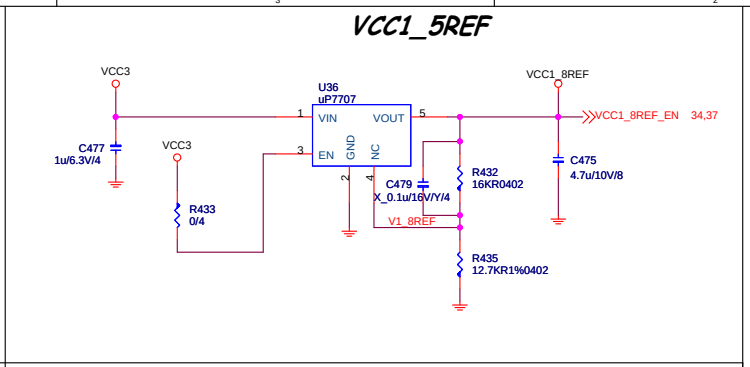

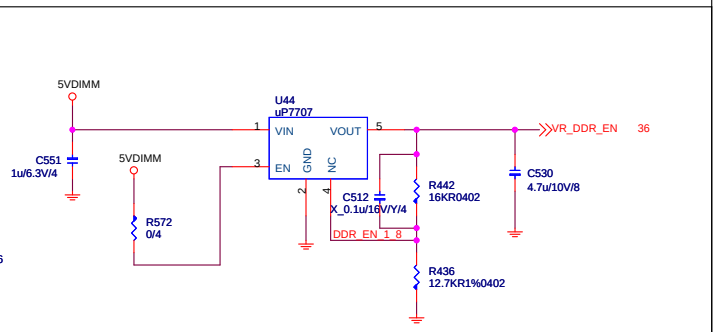

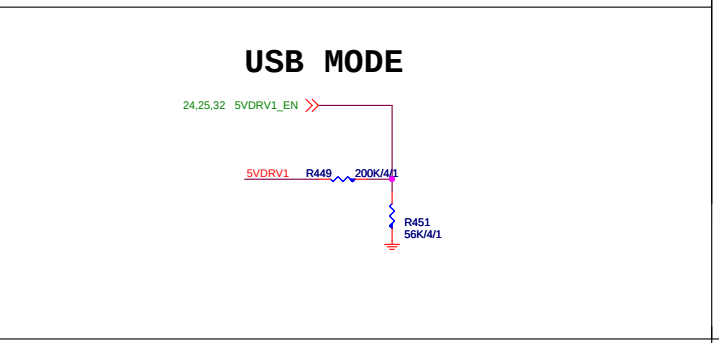

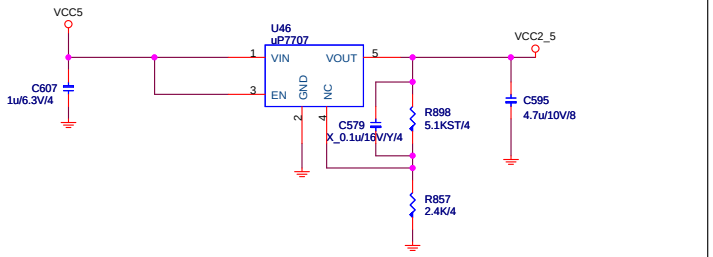

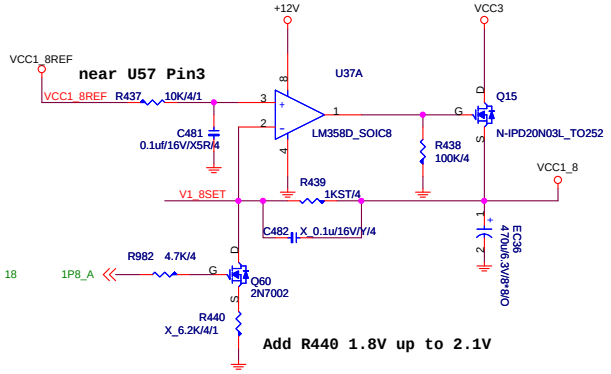

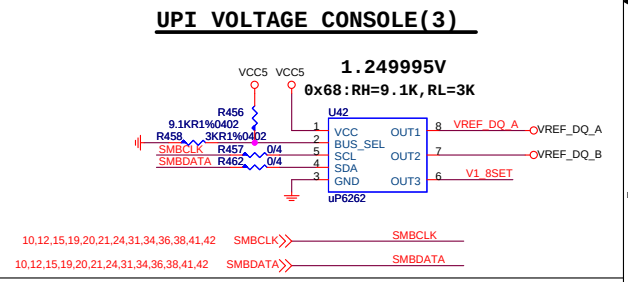

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Custom	ACPI controller UPI	0A

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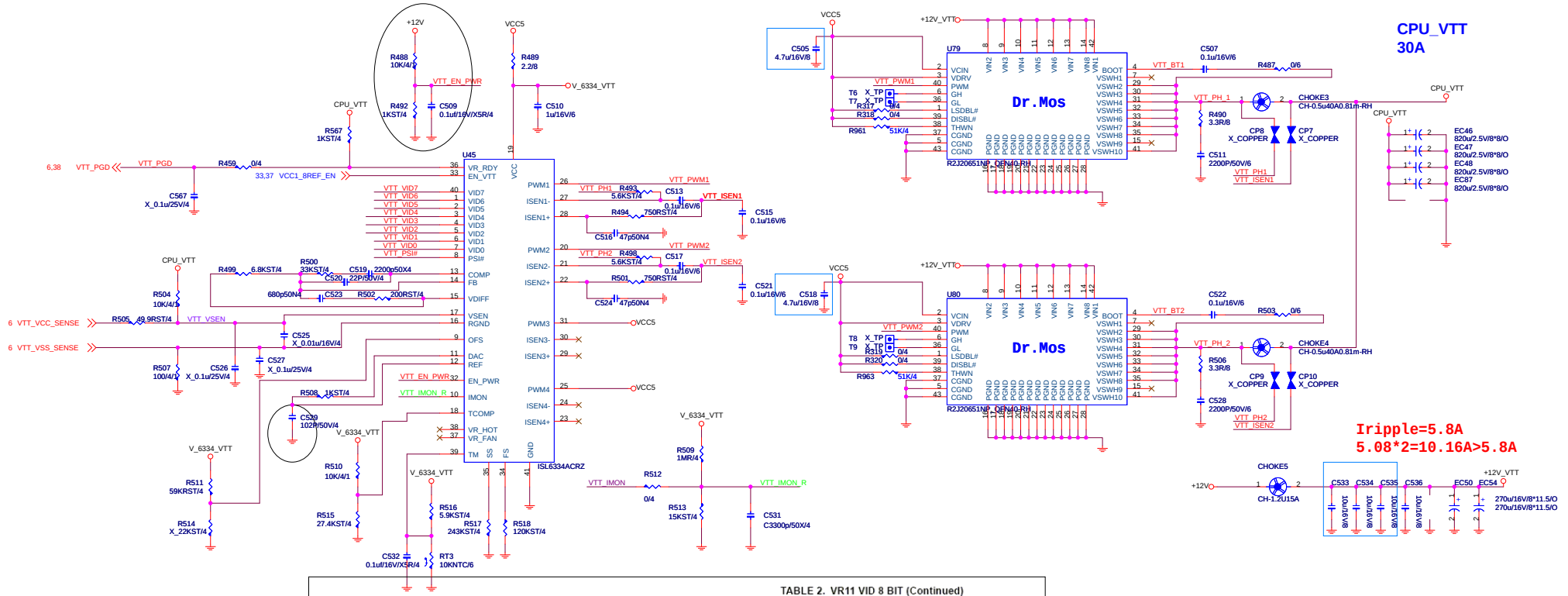
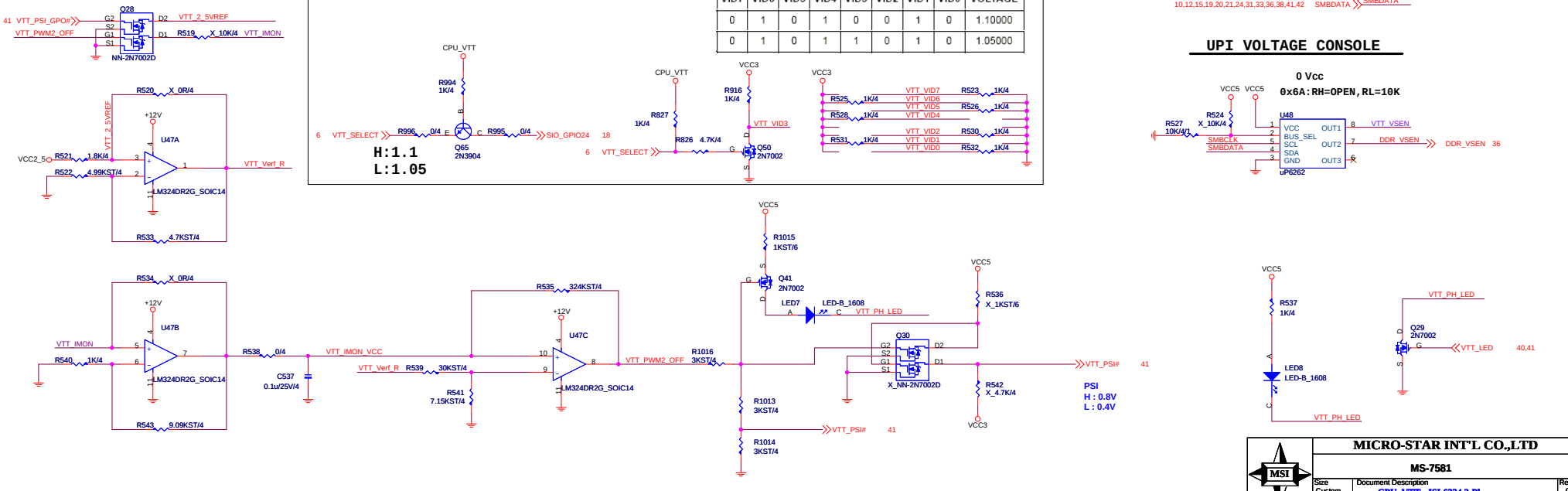
VTTPWRGD LEVEL SHIFT



VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	1	0	1	0	1.05000

TABLE 2. VR11 VID 8 BIT (Continued)



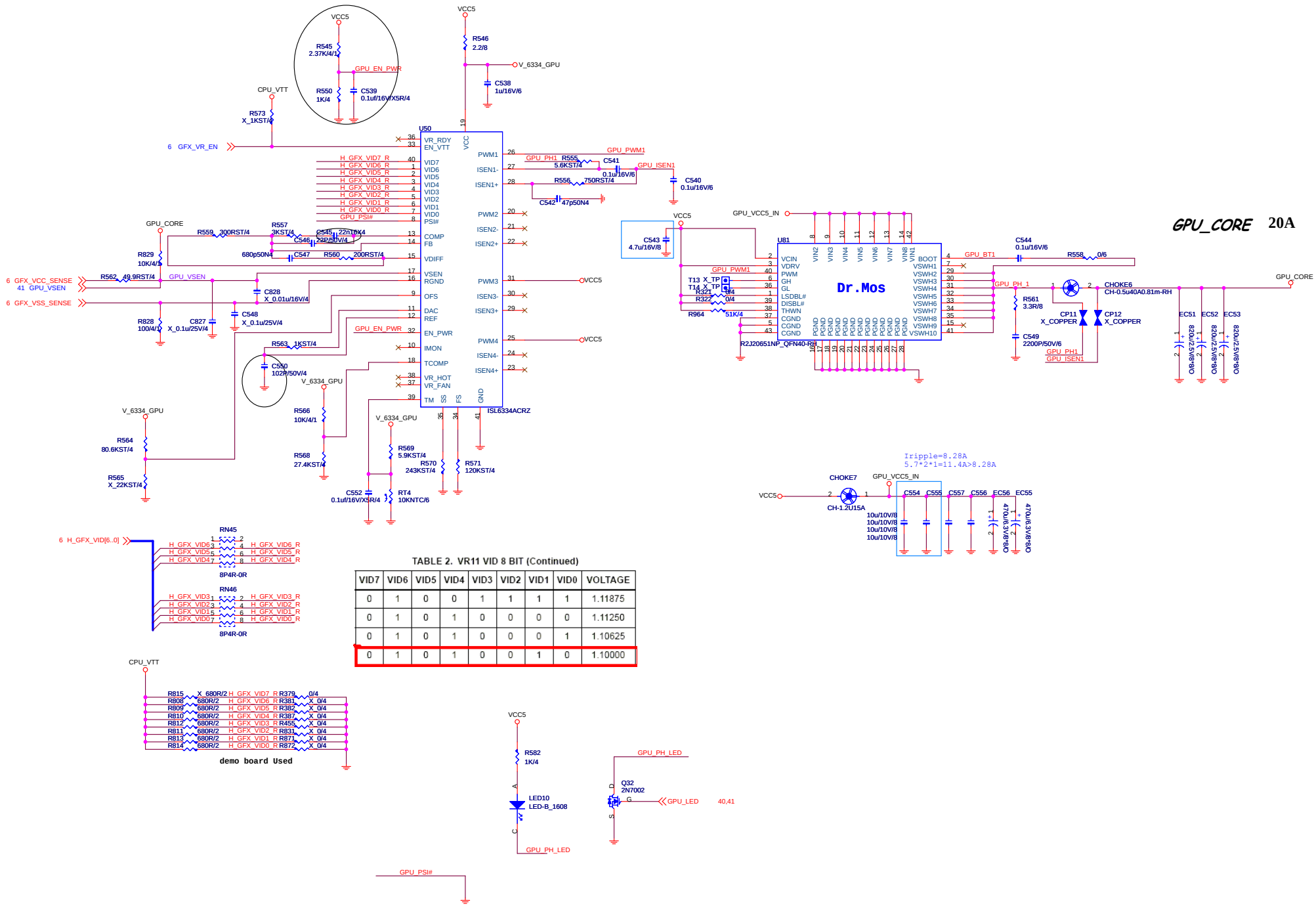


TABLE 2. VR11 VID 8 BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000

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TABLE 2. VR11 VID 8 BIT

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	1	0	0	1	0	1.50000

DDR3_1.5V
10.75A

1.8A*4+2.5A+0.75A=10.75A

U54 ISL6334ACRZ

U82 R2J20651NP

U83 R2J20651NP

Dr.Mos

CHOKE8 CH-1.2U15A

CHOKE9 CH-1.2U15A

CHOKE10 CH-1.2U15A

Irripple=2.63A
5.7*2*1=11.4A>2.63A

Place near NB VRM controller as closed as possible

CLOSED NB POWER PIN26

DDR Sensor I2C ADDR=66

U56 F75133S-LF

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

U77 uP7711
1.25V/2.9A

0.2075A*6=1.245A

PSI
H : 0.8V
L : 0.4V

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	MS-7581
Size: Custom	Document Description: DDR POWER - ISL6334 2-Phase
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PCH Core

6.5A

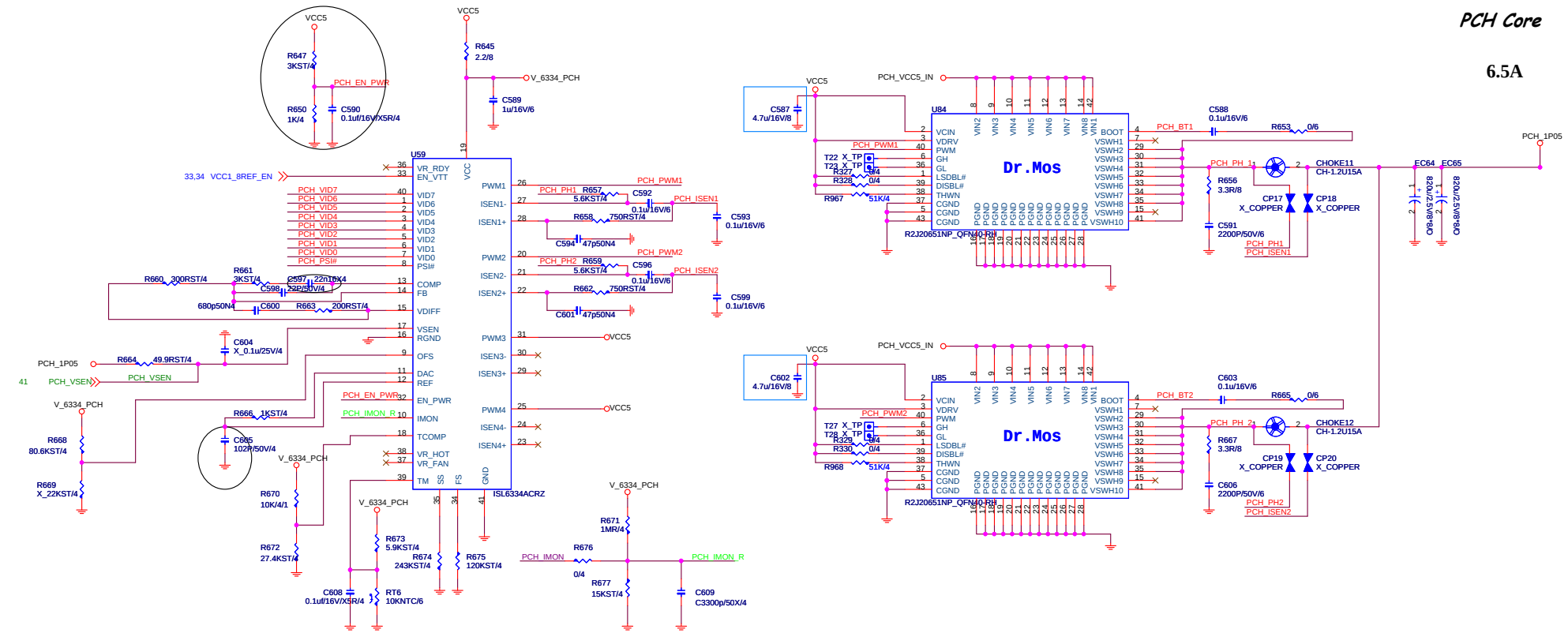
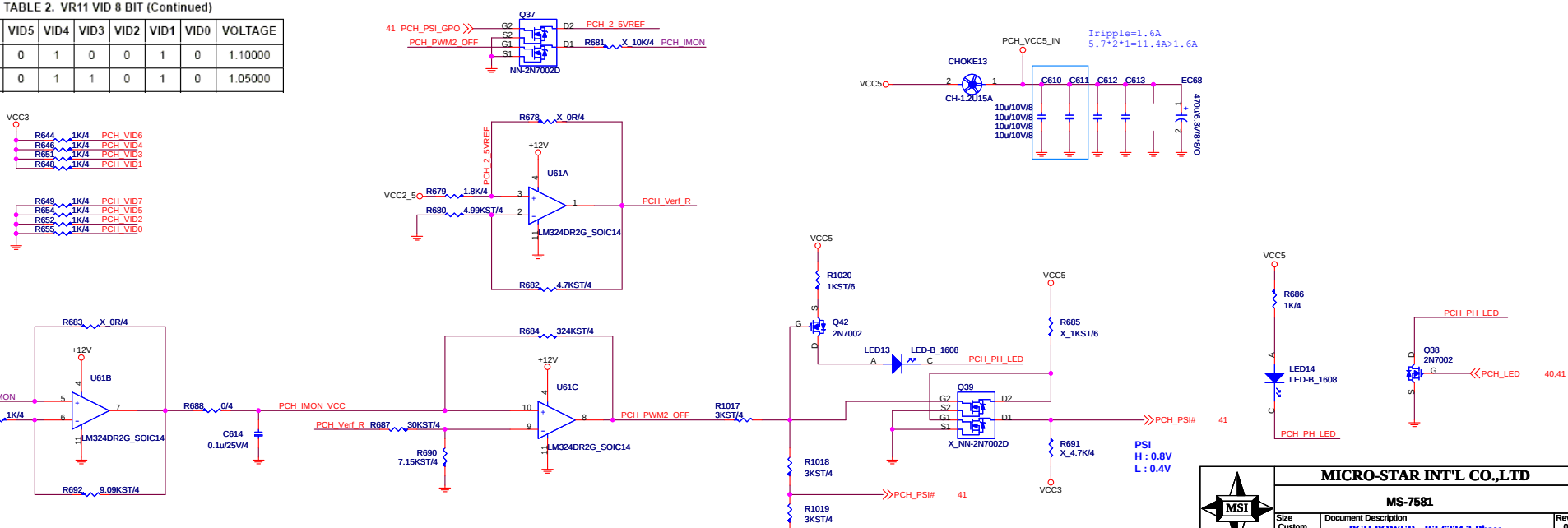


TABLE 2. VR11 VID 8 BIT (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	1	0	1	0	1.05000



MICRO-STAR INT'L CO.,LTD

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Size: Custom | Document Description: PCH POWER - ISL6334 2-Phase | Rev: 0A

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Up6208 VRD11.1 POWER CKT

POWER WATTAGE MONITOR

VRMPWRGD LEVEL SHIFT

CPU_VTT, VCCP, 3VSB, VCC3
R332 1K/4, R192 X_4.7K/4, R160 10K/4/1, R164 1KST/4
VRM_PGD_R, R191 4.7K/4, Q20 NN-CMKT3904, R167 100K/4, VRM_PGD 12,15
C95 X_0.1u/25V/4, C94 X_1u/6.3V/4

Delay 10us

3VSB, +12VIN
R824 6.2K/4/1, R484 4.7K/4, R825 1K/4, R485 10K/4/1
Q61 2N3904, VTT_ENABLE
6,34 VTT_PGD, R483 10K/4/1, Q51 2N3904, C506 1u/6.3V/4
C765 X_0.1uf/10V/X7R/4, C746 0.1uf/10V/X7R/4

CPU_VTT, R897 1K/4, CPU_VIDSEL
+12VIN, R693 9.1KR1%0402, R694 2.2R1%/6, VCC5, R695 1K/4
VRM_PGD_R, VTT_ENABLE, R696 1K/4, C615 0.01u/16V/4, C616 C0.1u16X, R697 1K/4

U63 (up6208)

Pin			
52	VTT		
50	PWRGD		
51	EN		
48	VCC		
49	GND		
32	ADDR		
53	VID7	H_VID7_R	
54	VID6	H_VID6_R	
55	VID5	H_VID5_R	
56	VID4	H_VID4_R	
57	VID3	H_VID3_R	
58	VID2	H_VID2_R	
59	VID1	H_VID1_R	
60	VID0	H_VID0_R	
61	VIDSEL	CPU_VIDSEL	
1	IMON	VCCP_IMON	
2	IMAX2	IMAX_R	
64	VOUT		
63	TB		
3	FBRTN		
4	SS		
7	COMP		
8	FB		
5	DACQ		
6	EAP		
9	OFS		
62	PSI#		
46	SDA		
47	SCL		
28	CSUMN		
29	CSUMP		
30	IMAX1		
31	RT		
45	PWM1	PWM1	39
44	PWM2	PWM2	39
43	PWM3	PWM3	39
42	PWM4	PWM4	39
41	PWM5	PWM5	39
40	PWM6	PWM6	39
39	PWM7	PWM7	39
38	PWM8	PWM8	39
37	PWM9		
36	PWMA		
35	PWMB		
34	PWMC		
33	GND		

Current sense

ISP1	R710 3KR1%0402	C626 C1u16X-RH	C627 C0.1u16X	PWM_SW_1	39,41
ISN12	R899 0/4			PWM_OUT12	39,41
ISP2	C630 C1u16X-RH	R713 3KR1%0402		PWM_SW_2	39,41
ISP3	R716 3KR1%0402	C634 C1u16X-RH	C635 C0.1u16X	PWM_SW_3	39,41
ISN34	R900 0/4			PWM_OUT34	39,41
ISP4	C637 C1u16X-RH	R719 3KR1%0402		PWM_SW_4	39,41
ISP5	R723 3KR1%0402	C640 C1u16X-RH	C641 C0.1u16X	PWM_SW_5	39,41
ISN56	R901 0/4			PWM_OUT56	39,41
ISP6	C644 C1u16X-RH	R725 3KR1%0402		PWM_SW_6	39,41
ISP7	R727 3KR1%0402	C647 C1u16X-RH	C648 C0.1u16X	PWM_SW_7	39,41
ISN78	R902 0/4			PWM_OUT78	39,41
ISP8	C649 C1u16X-RH	R731 3KR1%0402		PWM_SW_8	39,41

41

R847 4.7K/4

ISP1	R816 X_3KR1%0402	PWM_OUT12	
ISP2	R817 X_3KR1%0402	PWM_OUT12	
ISP3	R818 X_3KR1%0402	PWM_OUT34	
ISP4	R819 X_3KR1%0402	PWM_OUT34	
ISP5	R820 X_3KR1%0402	PWM_OUT56	
ISP6	R821 X_3KR1%0402	PWM_OUT56	
ISP7	R822 X_3KR1%0402	PWM_OUT78	
ISP8	R823 X_3KR1%0402	PWM_OUT78	

Voltage sense

6,41 CPU_VCC_SENSE, R707 0/4, C621 C0.1u16X
6 CPU_VSS_SENSE, C625 X_C0.1u16X, R711 100/4/1
6,41 CPU_VCC_SENSE, C628 X_22nf/16V/4
VCCP, R714 10K/4/1, C632 X_C0.1u16X
R708 0/4, C623 C1500p50X0402, R709 560R1%0402-RH
R712 0/4, C629 22nf/16V/4, R715 2K/4, C631 X_0.01u/16V/4
R718 X_2K/4, C636 C10p25N0402-RH-3, R720 15KST/4, C639 C6800p16X0402
C643 C470p50X0402, R722 0/4, R724 1K/4
6,18,41 VCCP_IMON, R726 2K/4, C645 X_0.01u/16V/4
41 PM_CPU, V2
C646 X_0.01u/16V/4, R728 0/4, R729 2K/4, RT X_10KNTC/6, R730 2.2KR1%0402
Closed CHOCK, V1
CPU_VTT, R732 X_4.7K/4
VCC5, R733 X_2K/4, OFS
IMAX_R, R735 2K/4, C650 X_0.01u/16V/4
6 VCCP_PSI#
10,12,15,19,20,21,24,31,33,34,36,41,42 SMBDATA, R736 0/4
10,12,15,19,20,21,24,31,33,34,36,41,42 SMBCLK, R737 0/4

OFS control

OFS, R976 4.7K/4, 41 OFS_CTL, Q59 2N7002, R734 X_2K/4

PWM routing

41 PWM_OUT

39,41 PWM_OUT12	R738 1R1%/6	R739 1K/4	C651 0.1u/25V/4, C652 C1u16X-RH
39,41 PWM_OUT34	R740 1R1%/6		
39,41 PWM_OUT56	R741 1R1%/6		
39,41 PWM_OUT78	R742 1R1%/6		
39,41 PWM_SW_1	R743 9.1KR1%0402		
39,41 PWM_SW_2	R744 9.1KR1%0402		
39,41 PWM_SW_3	R745 9.1KR1%0402		
39,41 PWM_SW_4	R746 9.1KR1%0402		
39,41 PWM_SW_5	R747 9.1KR1%0402		
39,41 PWM_SW_6	R751 9.1KR1%0402		
39,41 PWM_SW_7	R752 9.1KR1%0402		
39,41 PWM_SW_8	R756 9.1KR1%0402		

41 PWM_SW

R748 2K/4, C653 0.01u/16V/4, R749 22KR1%0402-RH-1

H_VID[7..0]

6 H_VID[7..0]

RN43 8P4R-0R

H_VID7	H_VID7_R
H_VID6	H_VID6_R
H_VID5	H_VID5_R
H_VID4	H_VID4_R

RN44 8P4R-0R

H_VID3	H_VID3_R
H_VID2	H_VID2_R
H_VID1	H_VID1_R
H_VID0	H_VID0_R

CPU_VTT

R793 X_1K/4	H_VID7_R	R792 1K/4	
R795 X_1K/4	H_VID6_R	R794 1K/4	
R797 1K/4	H_VID5_R	R796 X_1K/4	
R799 X_1K/4	H_VID4_R	R798 1K/4	
R801 1K/4	H_VID3_R	R800 X_1K/4	
R803 1K/4	H_VID2_R	R802 X_1K/4	
R805 1K/4	H_VID1_R	R804 X_1K/4	
R807 1K/4	H_VID0_R	R806 X_1K/4	

demo board Used

Power stage

POWER1, PWRCONN8P_BLACK-RH-2
GND, +12V, MEC1
+12VIN, L16 CH-1.2U25A-LF
C655 C658 0.01u/16V/4, X_10u/12Y, 12V1
CP21 X_COPPER, CP22 X_COPPER, 12V2
EC69 EC70 470U/16V/O, EC71 EC84 270U/16V/8*11.5/O, EC72 270U/16V/8*11.5/O, C659 X_10u/16V/12
12VIN

Output monitor

VCC5, C619 X_100p/16V/4, C620 X_100p/16V/4, C617 0.1uf/10V/X7R/4
V1, U62B, LMV772MAX,SOIC8, R700 110K/4/1, R701 10K/4/1, R704 10K/4/1, R706 X_10KR/2
V2, U62A, LMV772MAX,SOIC8, Vout1, R703 110K/4/1, R705 X_10KR/2

C622 0.1uf/10V/X7R/4
C624 0.1u/25V/4, C633 X_0.1uF/25V/4, C638 0.1u/25V/4
U64 LMP8270 (Vin+, Vin-, VCC, GND, Vout, NC, A1, A2)
12V1, 12V2, Vout2, R717 150KST/4, R721 X_150KST/4, C642 102P/50V/4

V1, V2 trace length不可拉太長,
LMV772MAX放在near PWM IC

C655 X_1u/25V/X/8
C656 X_1u/25V/X/8
C660 X_1u/25V/X/8
C661 X_1u/25V/X/8
C662 X_1u/25V/X/8
C663 X_1u/25V/X/8
C664 X_1u/25V/X/8
C665 X_1u/25V/X/8
C666 X_1u/25V/X/8

For Power team test only

MICRO-STAR INT'L CO.,LTD

MS-7581

Size	Document Description	Rev
Custom	VRD11.1 - UP6208 8-Phase	0A
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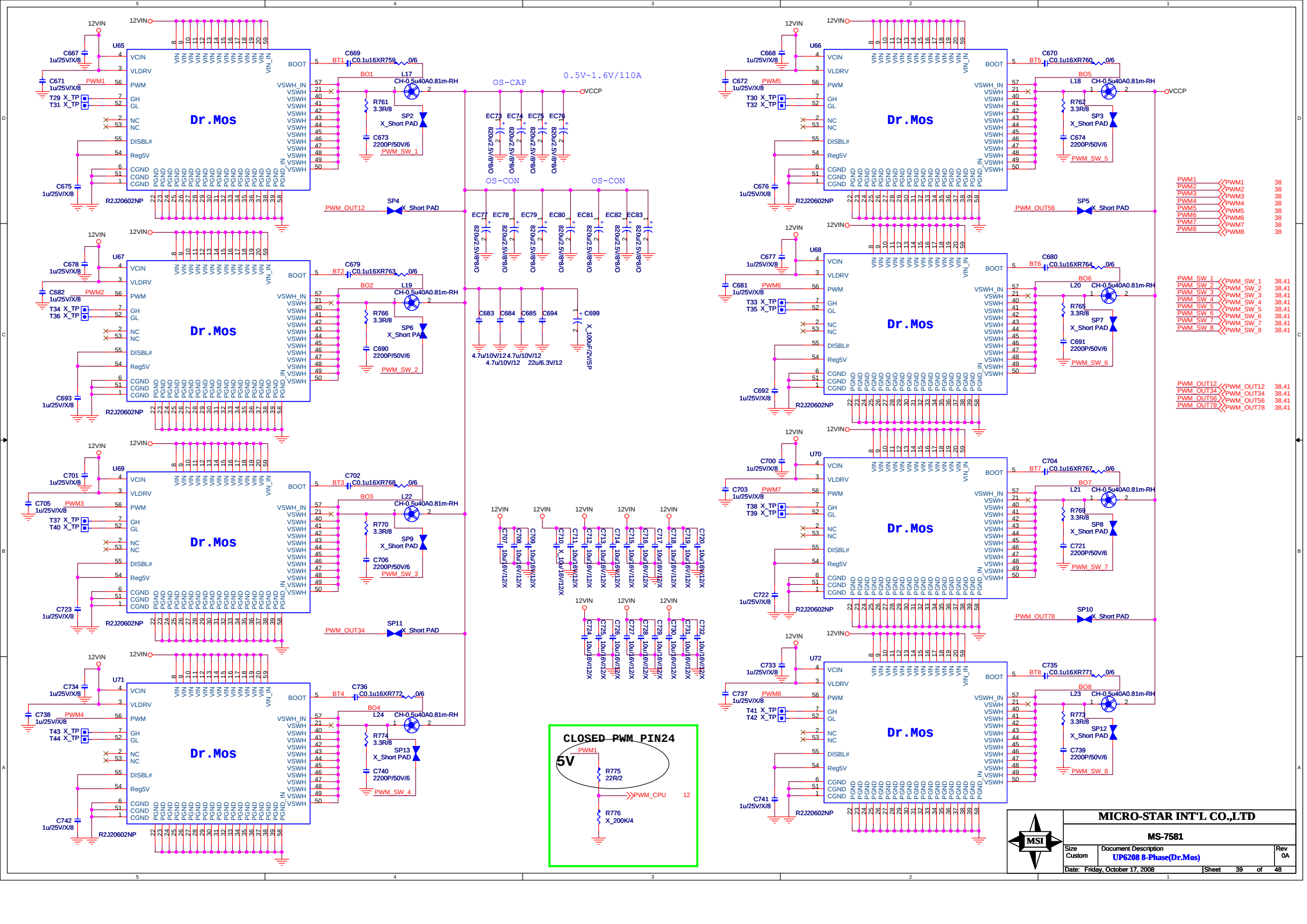
U65
U66
U67
U68
U69
U70
U71
U72
Dr.Mos
R2J20602NP
12VIN
VCCP
OS-CAP
OS-CON
0.5V~1.6V/110A
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
PWM7
PWM8
PWM_OUT12
PWM_OUT34
PWM_OUT56
PWM_OUT78
L17
L18
L19
L20
L21
L22
L23
L24
CH-0.5u40A0.81m-RH
SP2
SP3
SP4
SP5
SP6
SP7
SP8
SP9
SP10
SP11
SP12
SP13
X_Short PAD
PWM_SW_1
PWM_SW_2
PWM_SW_3
PWM_SW_4
PWM_SW_5
PWM_SW_6
PWM_SW_7
PWM_SW_8
CLOSED PWM PIN24
5V
R775
22R/2
R776
X_200K/4
PWM_CPU
MICRO-STAR INT'L CO.,LTD
MS-7581
UP6208 8-Phase(Dr.Mos)
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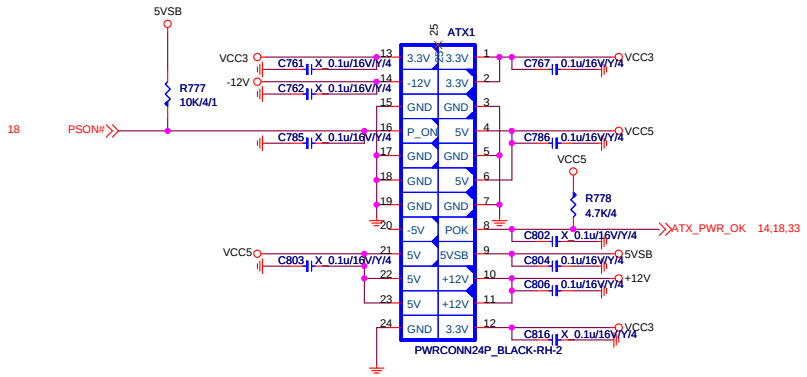
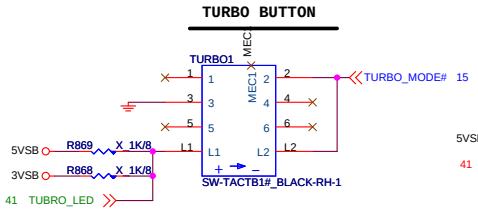
ATX POWER CONNECTOR

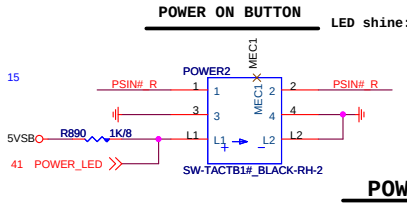


TURBO BUTTON



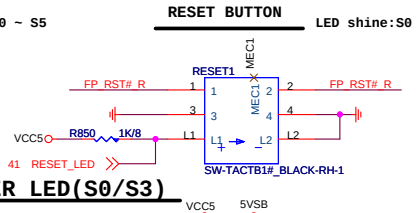
POWER ON BUTTON

LED shine:S0 ~ S5

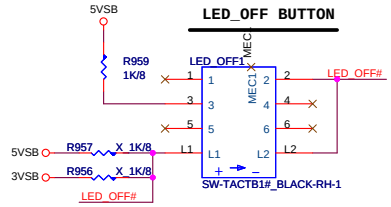


RESET BUTTON

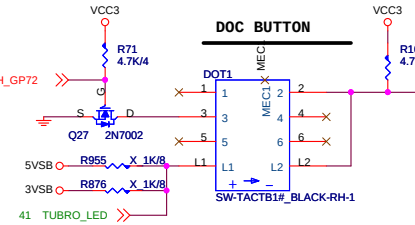
LED shine:S0



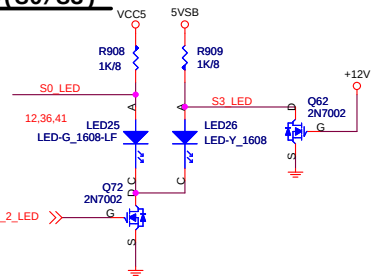
LED_OFF BUTTON



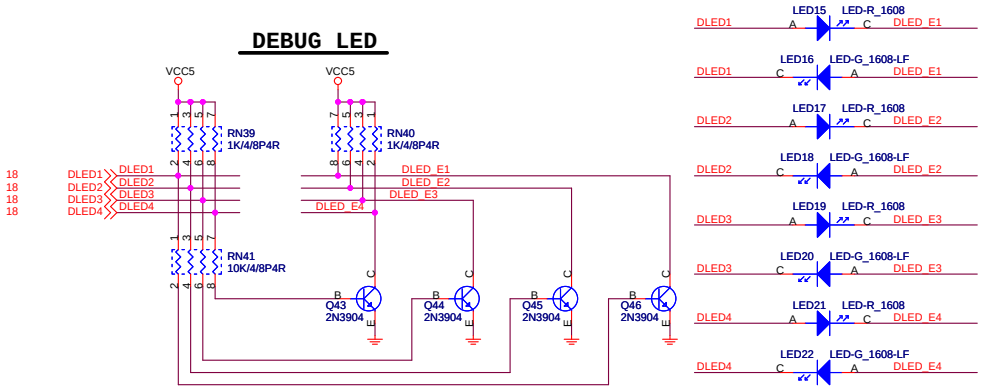
DOC BUTTON



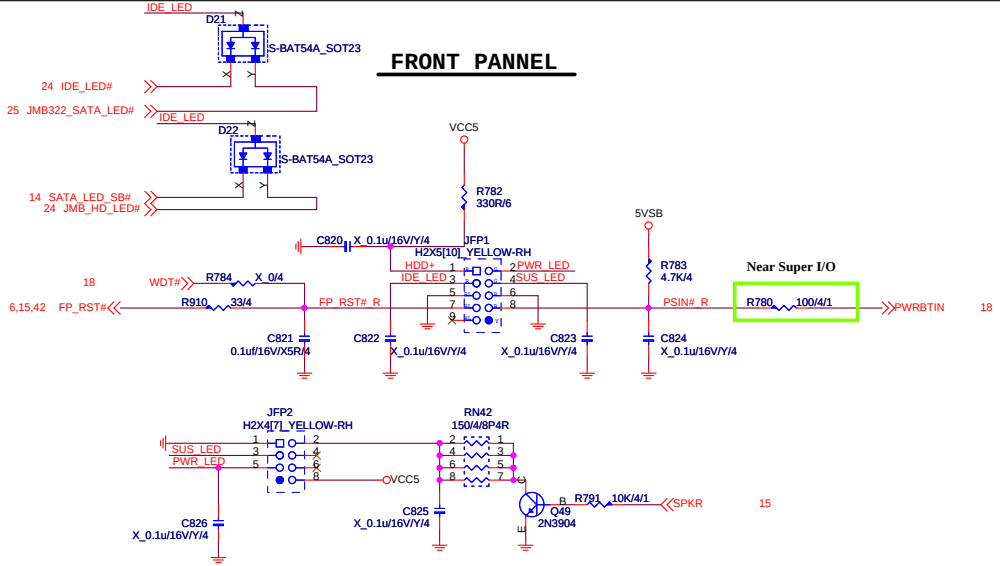
POWER LED(S0/S3)

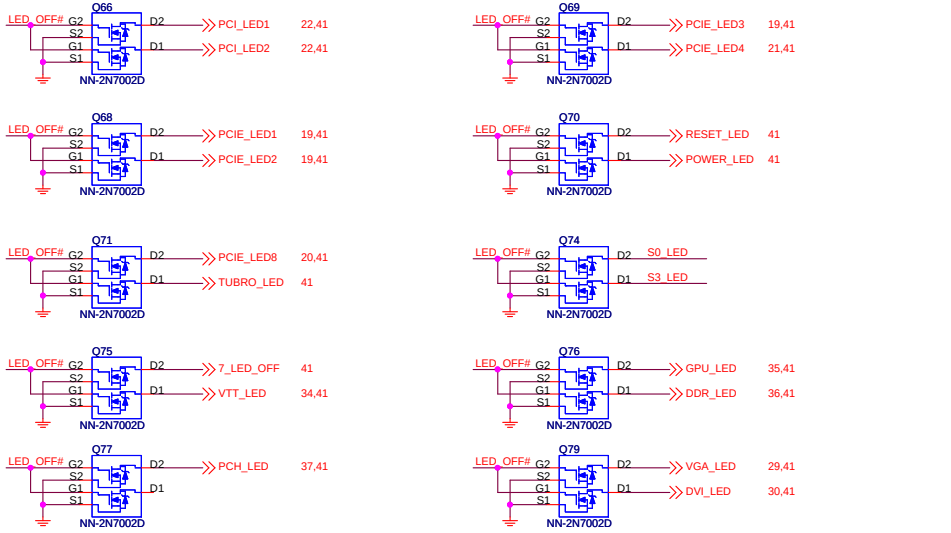


DEBUG LED

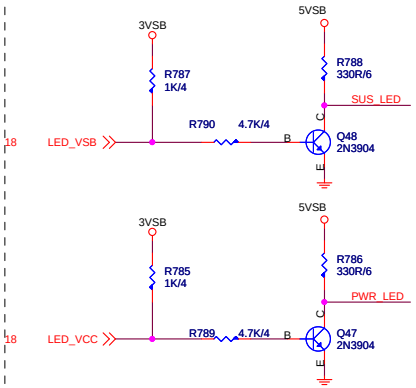


FRONT PANNEL

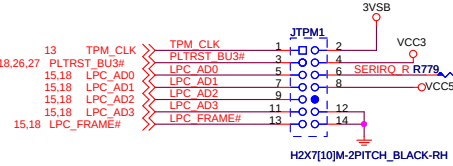




LED (for Fintek 71882)



TPM



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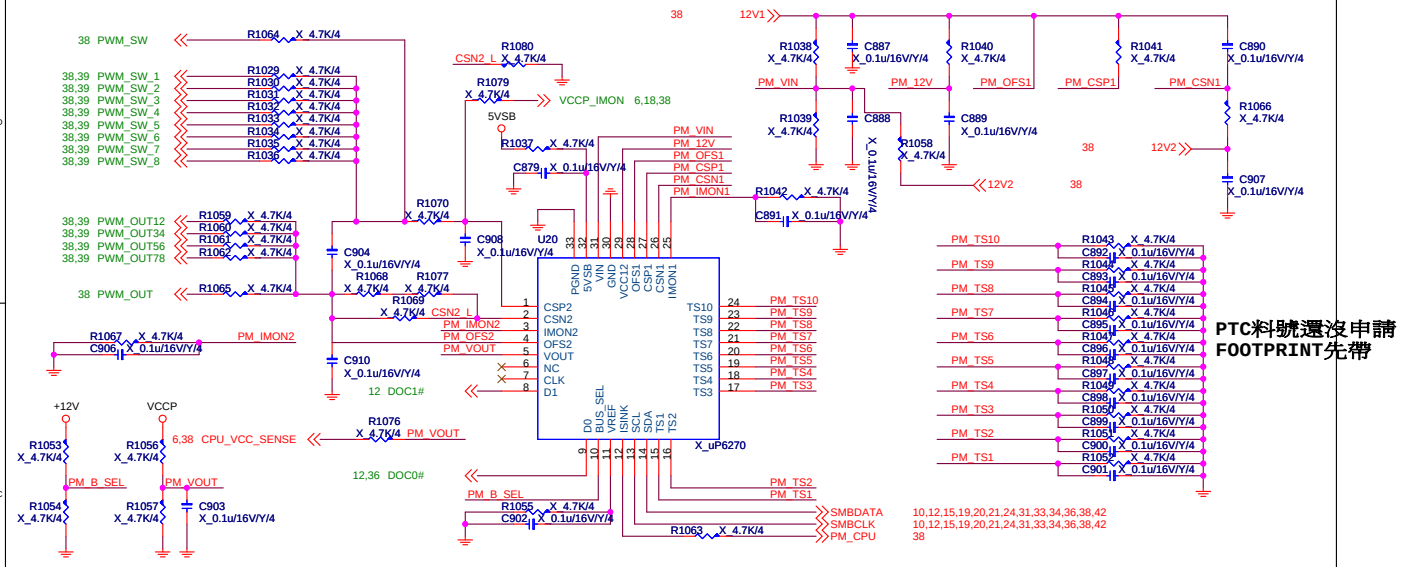
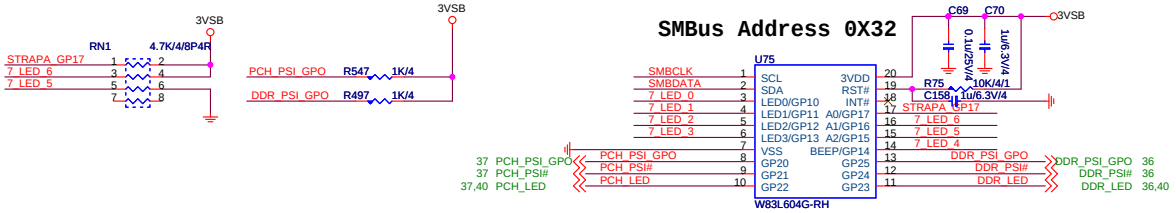
POWER METER

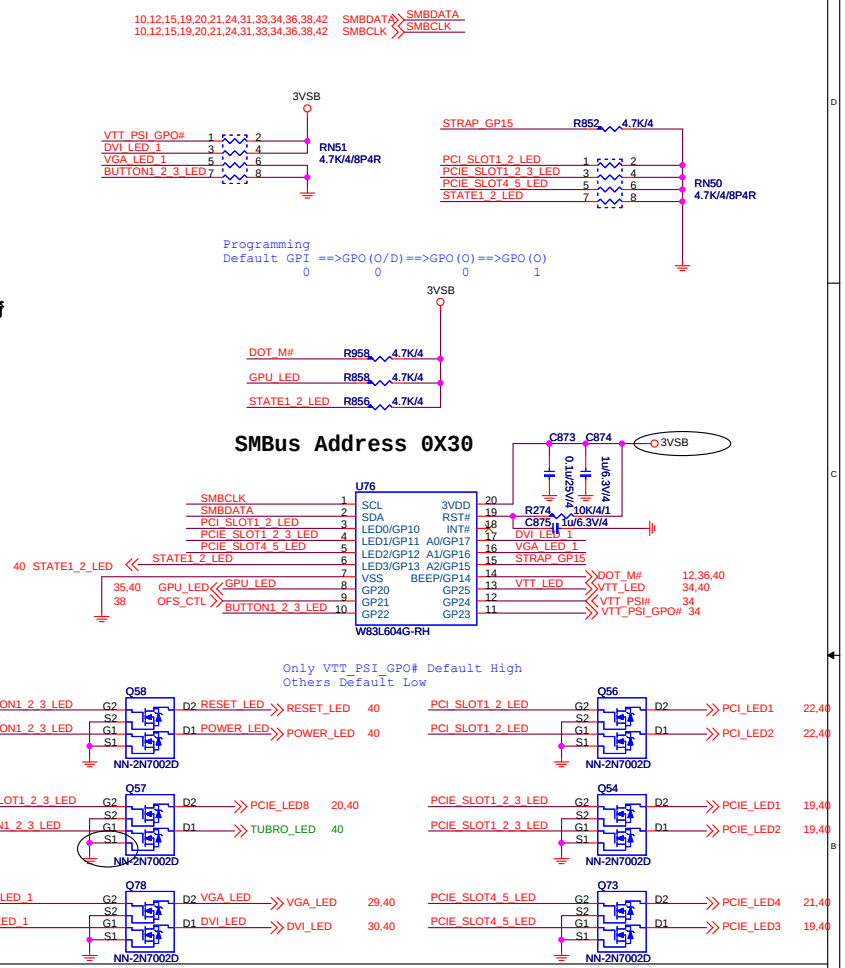


PTC料號還沒申請
FOOTPRINT先帶

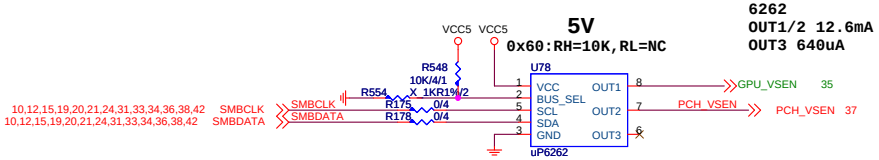
GPIO Controller - A VCORE / DDR / NB



GPIO Controller - B LED / VTT / PHASE6



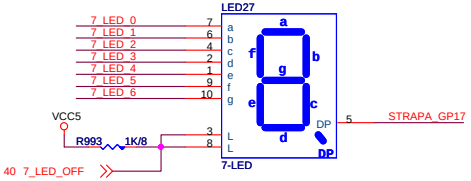
SM ADDRESS要重看

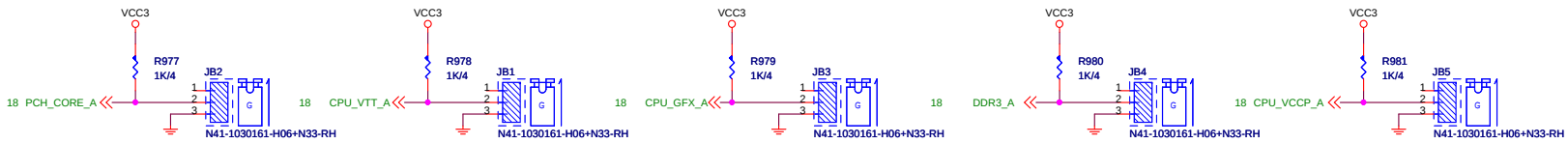


CPU_7段顯示器

PWM 1 PHASE:	PWM 2 PHASE:	PWM 4 PHASE:
7_LED_0=high	7_LED_0=low	7_LED_0=high
7_LED_1=low	7_LED_1=low	7_LED_1=low
7_LED_2=low	7_LED_2=high	7_LED_2=low
7_LED_3=high	7_LED_3=low	7_LED_3=high
7_LED_4=high	7_LED_4=low	7_LED_4=high
7_LED_5=high	7_LED_5=high	7_LED_5=low
7_LED_6=high	7_LED_6=low	7_LED_6=low

PWM 8 PHASE:7_LED_0~6 will to low





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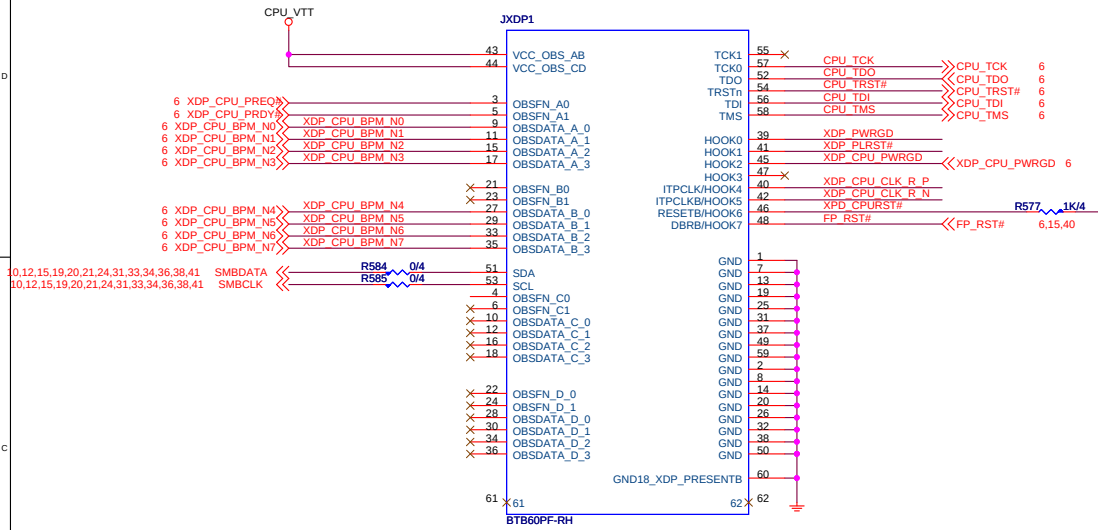
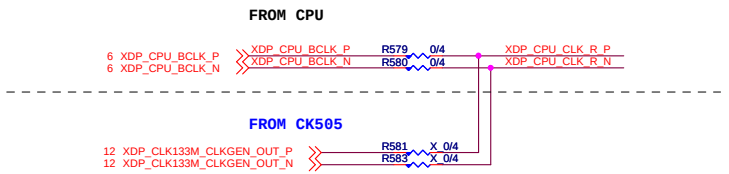
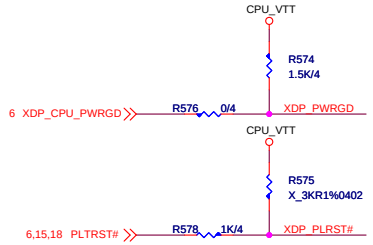
Reserve debug port 5020



CPU XDP CLOCK



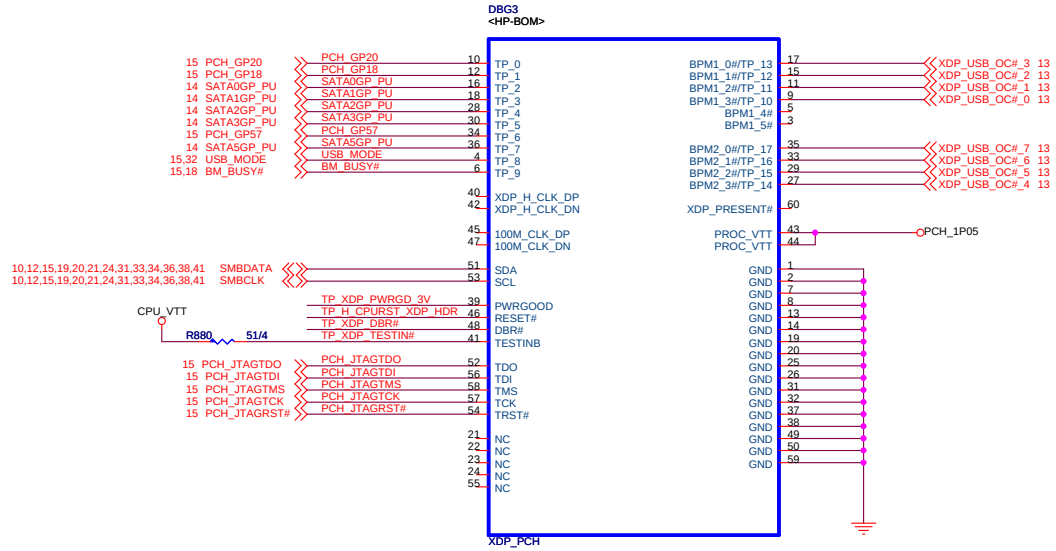


Simulation

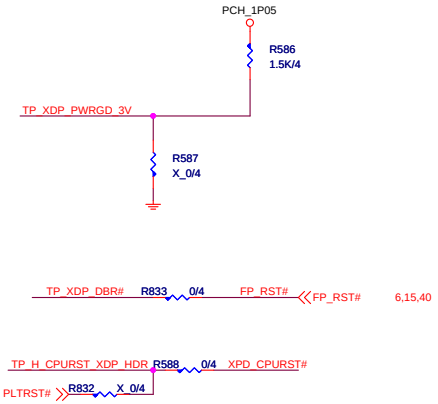
Optical Fiducial Marks-120

Optical Fiducial Marks-100

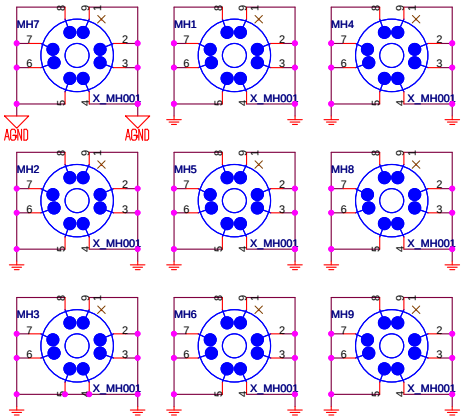
PCH XDP



PCH XDP PWRGD/RESET



Mounting Holes



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU/PCH XDP	Rev: 0A
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